MLX73290-A

300 to 960MHz Multi-channel Transceiver With 3DLF Low Power Interface

Features and Benefits

- 3DLF interface for low power wake-up
- Backup mode for battery less operations
- RSSI information for LF and RF interfaces
- LF/ RF intelligent self-polling modes for low power operations
- Multi-band frequency coverage from 300MHz up to 960MHz
- Modulation schemes supported: (G)FSK, (G)MSK, OOK
- Transmitter power of -20 to 13dBm, 64 steps
- Receiver sensitivity of -120dBm (FSK, 433MHz, 15kHz CHBW)
- Supply voltage range of 2.1 to 3.6V
- PLL synthesizer with 60Hz resolution
- Channel filter bandwidth of 9 to 600kHz
- Data rate of 0.3 to 250kbps (GFSK)
- Frequency deviation up to 125kHz
- 32MHz crystal frequency
- SPI interface with embedded FIFO, 256bytes for RF and 8bytes for LF interfaces 4 programmable GPIO ports
- 32L QFN5x5 package
- Conform to EN 300 220, DASH7, FCC part 15, Japan ARIB STD-T67, Korean and other standards

Application Examples

- Low-power tracking systems
- Secure access systems
- Passive Keyless Entry / Start (PKES)

Ordering Code

Product	**Temperature**	**Package**	**Option**	**Packaging Form**
MLX73290	R	LQ	ABA-000	RE or TU
Legend:	R for -40°C to 105°C	LQ for 32L QFN5x5		RE for reel (5000 pcs.)

Introduction

The MLX73290-A combines a highly integrated Radio Frequency transceiver for long range, high speed communication and a 3 dimensional low frequency interface (3DLF) for low power wake-up. This unique combination makes the MLX73290-A suitable for applications requiring a very low power wake-up function together with long range, high speed RF feedback.

The transceiver part allows for multi-channel operation including frequency hopping in the European bands (433MHz and 868MHz) as well as in North America or Asia bands (315MHz or 915MHz). The output power, frequency channel, modulation type and frequency deviation are programmable. Thanks to the high frequency resolution and phase noise performance of its fractional-N PLL, the MLX73290-A is fit for narrow-band operation. There are two selectable modulation schemes: binary on-off keying (OOK) and binary frequency shift keying (FSK) as well as their Gaussian filtered versions. The low-IF receiver part comprises fully digital demodulation and self-polling features together with channel scanning and built-in packet recognition.

The 3DLF interface features an automatic and programmable wake-up algorithm together with an integrated data decoder to receive the payload. Monitoring independently the RSSI information from the 3-axis LF front-ends allows precise monitoring of the received LF field. Thanks to its internal rectifier, power management and load modulator, the MLX73290-A is capable of battery-less LF RFID tag operation.

1 Glossary of Terms

3DLF	3 Dimensional Low Frequency interface
ADC	Analog to Digital Converter
PLL	Phase locked loop
POR	Power-on reset
MCU	External host microcontroller

2 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage	V_{DD}	0 to 4	V
Operating Temperature Range	T_A	-40 to 105	°C
Storage Temperature Range	T_S	-55 to 125	°C
ESD Sensitivity (HBM)	V_{ESD}	±2	kV
ESD Sensitivity (CDM)	V_{ESD}	±0.5	kV

Table 1: Absolute maximum ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3 Pin Definitions and Pin-out

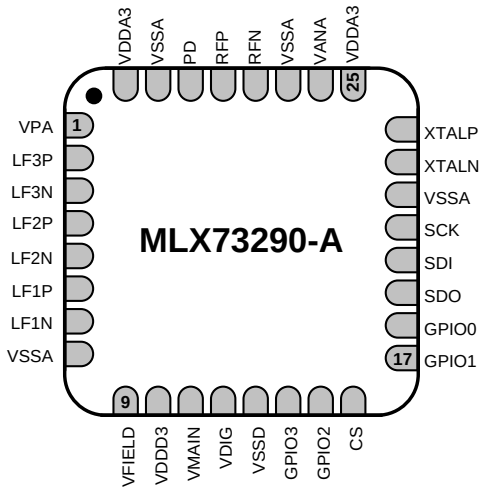


Figure 1: Pin-out of MLX73290-A

Pin №	Name	Type	Function
1	VPA	Supply	Supply of PA
2	LF3P	Analog	LF Positive input 3
3	LF3N	Analog	LF Negative input 3
4	LF2P	Analog	LF Positive input 2
5	LF2N	Analog	LF Negative input 2
6	LF1P	Analog	LF Positive input 1
7	LF1N	Analog	LF Negative input 1
8	VSSA	Ground	Analog Ground
9	VFIELD	Analog	Energy harvesting input
10	VDDD3	Supply	Battery supply (dedicated to power switch)
11	VMAIN	Supply	Power switch output for host MCU
12	VDIG	Regulated supply	Digital voltage regulator output
13	VSSD	Ground	Digital Ground
14	GPIO3	Analog/Digital	General Purpose IO3
15	GPIO2	Analog/Digital	General Purpose IO2
16	CS	Digital	SPI Chip Select
17	GPIO1	Analog/Digital	General Purpose IO1
18	GPIO0	Analog/Digital	General Purpose IO0
19	SDO	Digital	SPI Slave Data Output
20	SDI	Digital	SPI Slave Data Input
21	SCK	Digital	SPI Clock
22	VSSA	Ground	Analog Ground
23	XTALN	Analog	Crystal negative input
24	XTALP	Analog	Crystal positive input
25	VDDA3	Supply	Analog supply
26	VANA	Regulated supply	Analog voltage regulator output
27	VSSA	Ground	Analog Ground
28	RFN	RF analog	RF port - positive
29	RFP	RF analog	RF port - negative
30	PD	RF analog	RF Power Detector
31	VSSA	Ground	Analog Ground
32	VDDA3	Supply	Analog Supply
EP	VSSA	Exposed pad	Analog Ground to be connected to GND on PCB

Table 2: Pin definitions

4 Electrical Specifications

4.1 Normal operating conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{DD}		2.1	3.0	3.6	V
Operating temperature (R)	T_A	R version	-40	27	105	°C
Input low voltage (CMOS)	V_{IL}	Digital pins	-	-	0.3 * V_{DD}	V
Input high voltage (CMOS)	V_{IH}	Digital pins	0.7 * V_{DD}	-	-	V

Table 3: Electrical specifications

4.2 General Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Timers						
Uncalibrated RC Oscillator	f_{RCclk}		19	32	35	kHz
Calibrated RC Oscillator	$f_{RCclkCal}$		-	15.6	-	kHz
General purpose ADC						
Effective Number Of Bit	ENOB		-	10	-	bit
Sample Rate	SR		4	-	16	kS/s
Temperature sensor						
Sensitivity	$temp_{sens}$		-	-1.6	-	mV/°C
Offset	$temp_{off}$	25°C	-	750	-	mV

Table 4: General characteristics

4.3 RF Characteristics

Operating Conditions T_A = -40°C to 105°C, V_{DD} = 2.1V to 3.6V (unless otherwise specified)
Typical values at T_A = 25°C and V_{DD} = 3.0V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
Frequency Range	$f_{RF,band1}$	BAND_SEL[1:0] = 0	299	-	331	MHz
	$f_{RF,band2}$	BAND_SEL[1:0] = 1	425	-	480	
	$f_{RF,band3}$	reserved for future use	-	-	-	
	$f_{RF,band4}$	BAND_SEL[1:0] = 3	850	-	960	
Operating currents						
Sleep mode	I_{SLEEP}	deep sleep	-	200	-	nA
		RCO on	-	400	-	
RF Receive mode	$I_{RX,315MHz}$	100kbps, FSK, NRZ	-	16	-	mA
	$I_{RX,433MHz}$		-	17	-	
	$I_{RX,868MHz}$		-	18	-	
	$I_{RX,915MHz}$		-	19	-	
RF Transmit mode	$I_{TX,315MHz}$	100kbps, FSK, NRZ, 0dBm	-	20	-	mA
		100kbps, FSK, NRZ, 10dBm	-	29	-	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
	$I_{TX,433MHz}$	100kbps, FSK, NRZ, 0dBm	-	21	-	
		100kbps, FSK, NRZ, 10dBm	-	31	-	
	$I_{TX,868MHz}$	100kbps, FSK, NRZ, 0dBm	-	30	-	
		100kbps, FSK, NRZ, 10dBm	-	42	-	
	$I_{TX,915MHz}$	100kbps, FSK, NRZ, 0dBm	-	31	-	
		100kbps, FSK, NRZ, 10dBm	-	43	-	
Transmitter						
Max. CW output power at highest power step	$P_{max,315MHz}$ $P_{max,433MHz}$ $P_{max,868MHz}$ $P_{max,915MHz}$	with 50Ω matching network	-20	13	-	dBm
Spurious emissions < 1GHz	P_{spur}	Complies with EN 300 220 , FCC part 15and ARIB	-	-	-54	dBm
Spurious emissions > 1GHz			-	-	-30	dBm
Optimum impedance of matching network	R_{OUT}	single ended at output, Pout=13dBm		50		Ω
Receiver						
FSK receiver sensitivity 2.4kbps NRZ FSK Δf=±4kHz BW=15kHz, BER=10^{-3}	$P_{FSK,315MHz}$	315MHz	-	-120	-	dBm
	$P_{FSK,433MHz}$	433MHz	-	-120	-	dBm
	$P_{FSK,868/915MHz}$	868/915MHz	-	-116	-	dBm
OOK receiver sensitivity 2.4kbps NRZ BW=15kHz, BER=10^{-3}	$P_{OOK315MHz}$	315MHz	-	-115	-	dBm
	$P_{OOK433MHz}$	433MHz	-	-115	-	dBm
	$P_{OOK868/915MHz}$	868/915MHz	-	-114	-	dBm
Image rejection	IMR	after IQ calibration	40	50	-	dB
		w/o IQ calibration		25		
IF frequency	f_{IF}		-	fc/64	-	kHz
Channel filter bandwidth (digital)	CHBW	programmable	9	-	600	kHz
Input intercept point	IIP3	at max. gain		-28		dBm
Adjacent channel rejection	ACR	9kHz CHBW, (G)FSK	-	46	-	dB
Blocking	BLK	2MHz offset (50kHz CHBW)	-	52	-	dB
		10MHz offset (50kHz CHBW)	-	71	-	dB
Timings						
PA ramp up/down duration		programmable	0	-	192	µs
Channel switching time	t_{switch}	max frequency step	-	-	300	µs
RX/TX turn-around time	Δt_{RXTX}		-	-	50	µs
Sleep to RX on time	t_{RX}	programmable	200	-	-	µs
Sleep to TX on time	t_{TX}	programmable	200	-	-	µs
Modulator and data rate						
FSK deviation	Δf	Programmable in steps	-	-	±125	kHz
GFSK normalized BW	BT	fixed	-	0.5	-	
OOK modulation depth	M_{OOK}	100% modulation	70	80	-	dB
Data rate	BR_{FSK}	NRZ coding FSK	0.15	-	250	kbps
	BR_{OOK}	NRZ coding OOK	0.15	-	50	kbps
Synthesizer						
Phase noise	N_{PH_10kHz}	@ 10kHz offset	-	-	-94	dBc/Hz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
	N_{PH_1MHz}	@ 1MHz offset	-	-	-110	dBc/Hz
Frequency resolution	f_{RES}		57	61	65	Hz
RX/TX switching time	Δt_{RXTX}		-	-	50	µs
RX or TX frequency change			-	-	15	µs
Crystal oscillator						
Crystal oscillator frequency	f_0		30	32	34	MHz
Crystal oscillator start-up time	$t_{ROstart}$		-	0.8	1	ms
Recommended crystal specification						
Crystal frequency accuracy	Δf_0		-	-	±30	ppm
Load capacitance (differential)	C_L	Recommended for ext. crystal	8	12	15	pF
Static capacitance	C_0	Recommended for ext. crystal	-	-	5	pF
Maximum Drive Level	MDL	Recommended for ext. crystal	-	-	100	µW
Equivalent series resistance	R_1	Recommended for ext. crystal	-	-	70	Ω

Table 5: RF characteristics

4.4 LF Characteristics

Operating Conditions T_A = -40°C to 105°C, V_{DD} = 2.1V to 3.6V (unless otherwise specified)
Typical values at T_A = 25°C and V_{DD} = 3.0V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
LF frequency range	F_{LF}		115	-	140	kHz
LF Antenna Quality factor	Q_{ANT}		-	-	12	
Internal capacitance trimming	C_{BANK}		0	-	94.5	pF
Internal capacitance trimming	C_{STEP}		-	1.5	-	pF
Sensitivity	S_{ENS}		-	0.7	1	mVpp
Data-rate in RX/TX modes	D_R	Manchester encoding/decoding	-	f_{LF}/32	-	kbps
Operating currents						
Total current consumption during standby period	$I_{STANDBY}$	RCO running	-	730	-	nA
Current consumption during listen period	I_{LISTEN}		3.0	5	8.0	µA
Total current consumption during header detection	I_{HEADER}		10	-	31	µA
Total current consumption in RSSI mode	I_{RSSI}		121	-	130	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Average current consumption in scan mode	I_{avg}	f_{RCO} = 32kHz Register Tstandby [3:0] "0000" (3*t_{RCO}) "0001" (5*t_{RCO}) "0010" (4*t_{RCO}) "0011" (8*t_{RCO}) "0100" (6*t_{RCO}) "0101" (14*t_{RCO}) "0110" (10*t_{RCO}) "0111" (26*t_{RCO}) "1000" (18*t_{RCO}) "1001" (50*t_{RCO}) "1010" (34*t_{RCO}) "1011" (98*t_{RCO}) "1100" (66*t_{RCO}) "1101" (194*t_{RCO}) "1110" (130*t_{RCO}) "1111" (OFF)	-	6.1 5.5 5.8 5.0 5.3 4.5 4.8 4.0 4.2 3.7 3.8 3.4 3.6 3.3 3.4 -	-	µA
Timings						
Listen time	T_{LISTEN}	f_{RCO} = 32kHz	-	156.25	-	µs
Standby time in scan mode	$T_{STANDBY}$	f_{RCO} = 32kHz Register Tstandby [3:0] "0000" (3*t_{RCO}) "0001" (5*t_{RCO}) "0010" (4*t_{RCO}) "0011" (8*t_{RCO}) "0100" (6*t_{RCO}) "0101" (14*t_{RCO}) "0110" (10*t_{RCO}) "0111" (26*t_{RCO}) "1000" (18*t_{RCO}) "1001" (50*t_{RCO}) "1010" (34*t_{RCO}) "1011" (98*t_{RCO}) "1100" (66*t_{RCO}) "1101" (194*t_{RCO}) "1110" (130*t_{RCO}) "1111" (OFF)	-	93.8 156.3 125.0 250.0 187.5 437.5 312.5 812.5 562.5 1562.5 1062.5 3062.5 2062.5 6062.5 4062.5 -	-	µs
RSSI						
RSSI range input	R_{RSSI_IN}		1	-	1000	mVpp
RSSI range output	R_{RSSI_OUT}		0.	-	0.83	V
Effective Number Of Bit	ENOB	General purpose ADC	-	10	-	bit
RSSI settling time	R_{RSSI_SET}		-	-	500	µs
Battery backup characteristics						
External capacitor	REC_{CAP}		-	10	-	µF
Start-up time	REC_{START}	with 10uF on Vfield	4	-	40	ms
Load current	REC_{LOAD}		3	5	10	mA
Output voltage	REC_{VOUT}		-	-	3.6	V
Modulator resistance	R_{ON}		-	10	25	Ω

Table 6: LF characteristics

4.5 SPI Characteristics

Operating Conditions T_A = -40°C to 105°C, V_{DD} = 2.1V to 3.6V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SPI Clock Frequency	f_{SCLK}		-	1	10	MHz
SCK high time [1)]	t_{SCKH}	SCK ↑ to SCK ↓	40	-	-	ns
SCK low time [1)]	t_{SCKL}	SCK ↓ to SCK ↑	40	-	-	ns
SCK period [1)]	t_{SCK}	Between equal edges of SCK	100	-	-	ns
Setup time [1)]	t_{SU}	CS and SDI stable to SCK ↑	20	-	-	ns
Hold time [1)]	t_{HD}	SCK ↑ to CS or SDI changing	20		-	ns
SDO data delay [1)]	t_{SDO}	SCK ↓ to SDO stable	-	20	-	ns
Output enable delay [1)]	t_{OE}	SCK ↓ to SDO output enabled	-	20	-	ns
Output disable delay [1)]	t_{OD}	CS ↓ to SDO tri-state	-	50	-	ns

Table 7: SPI Characteristics

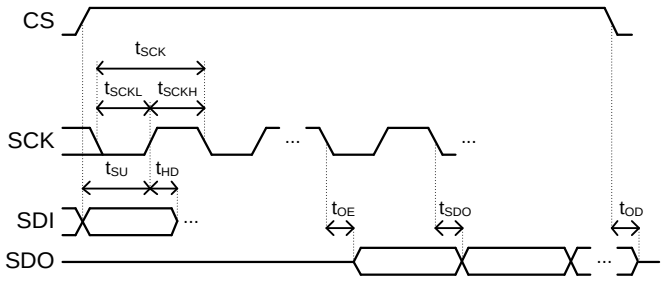


Figure 2: SPI timing specifications

5 Functional Description

5.1 Frequencies and standards

The MLX73290-A complies with the following frequency bands and radio standards.

freq. band [MHz]	max. ERP [dBm]	channel BW [kHz]	max. data rate [kbps]	Comment
300-330	-20	0.25% of center freq.	20 (OOK, FSK)	SRDs - FCC 15.231 Japan ULP Band
426-469 433-434 446-447	10 10 10	12.5 - 25 not defined 25	5 (FSK) 200 (OOK, FSK) 1.2 (FSK)	Japan (ARIB), Korea SRDs - EN 300 220, DASH7 Europe PMR, US FSR
863-870 902-928	14 -1	25 - 600 200 (typ.)	250 (OOK, FSK) 250 (OOK, FSK)	SRDs - EN 300 220 SRDs - FCC 15.249

5.2 Block diagram

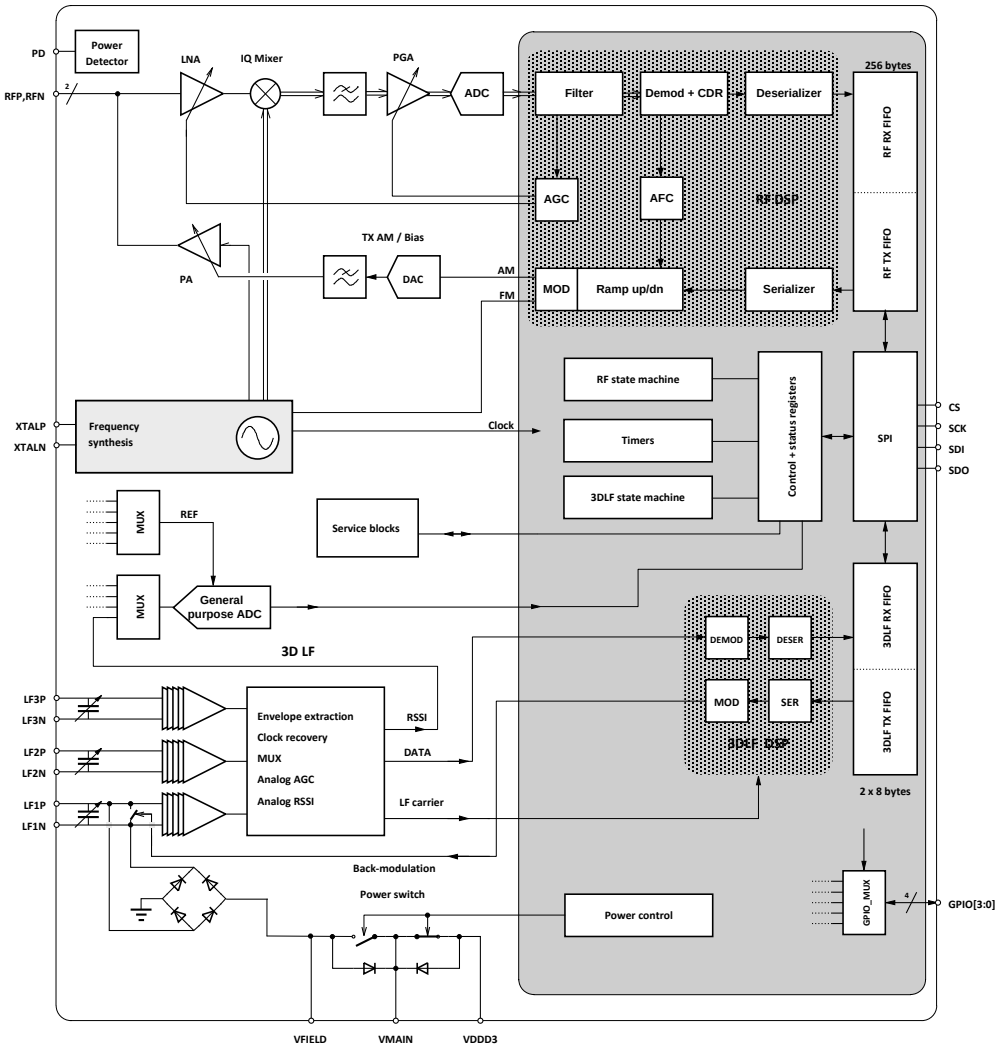


Figure 3: MLX73290-A block diagram (supply pins not shown)

5.3 Detailed description

The MLX73290-A combines a highly integrated Radio Frequency transceiver for long range communication and a 3 dimensional low frequency interface (3DLF) for low power wake-up. The device is fully programmable via its Serial Programming Interface (SPI), composed of four pins CS, SCLK, SDI and SDO. This allows for the configuration of the LF and RF transceiver interfaces (e.g. operating frequency, channels, frequency resolutions, output power, modulation types, frequency deviation, polling modes, LF wake-up state-machine …).

The frequency synthesizer of the RF transceiver uses a fractional-N PLL that can be modulated with a Σ-Δ modulator. The VCO is fully integrated. Frequency deviations of the crystal oscillator (XOSC) can be simply compensated by adding offsets to the control words of the Σ-Δ modulator. Gaussian filtering of the input data signal is implemented for FSK in order to provide a more narrow output spectrum.

The TX/RX RF port is a combined differential I/O port for half-duplex operation; the LNA and the PA are internally connected. The Power Amplifier (PA) output power is programmable in 64 steps ranging from -20 to +13 dBm and the ramp up/down time can be fine adjusted to limit transient emissions.

A low voltage detector automatically disconnects the PA if the supply voltage drops below a certain threshold value. This prevents the transmission of undesired frequencies when the battery reaches end of life.

In order to minimize the load of the host MCU, a packet handler takes care of formatting/pre-processing the data in both receive and transmit mode.

Self-polling is realized by an integrated timer with very low power consumption. The polling mode wakes up the receiver or transmitter after a programmable time and scans one or more frequency channels for valid data. It can also be used to transmit the same data in a periodic way.

The 3D Low Frequency interface, operates in the 125 kHz frequency range and is composed of three differential receive coil inputs, digitally controlled for very low power wake-up functionality. A dedicated state-machine can be configured to periodically scan for valid data on one of the three LF input and wake-up the external host MCU once a valid LF telegram has been successfully received.

A built-in power switch selects the power voltage from the battery or from the 3DLF interface (through an internal bridge rectifier). This is used in case of low battery, to supply the MLX73290-A and the host MCU with the power recovered from the interface LF-1.

Four General Purpose IOs (GPIO) are available to provide control information to the host MCU. Information like READY, BATTOK or RCO output is available after the Power On Reset (POR) of the device. Quantities of other information can be programmed on the GPIOs by the host MCU.

5.4 3DLF interface

A 3DLF interface has been integrated in the MLX73290-A for low power wake-up on a valid LF telegram. The operating frequency range is from 115 to 140 kHz. An autonomous state machine continuously scans for the presence of a valid header on one of the three LF interfaces to wake-up the external host MCU. Decoded LF data is stored in the internal 8-Bytes LF FIFO buffer. The 3DLF interface can also be configured in transparent mode, with the extracted clock and data available on GPIOs.

In order to reduce as much as possible the overall power consumption during scan activity, the 3DLF state-machine is using the internal uncalibrated RC oscillator f_{RCO} (between 18kHz and 42kHz with a typical value of 32kHz) as reference clock (f_{RCO} is available by default after POR on GPIO2).

Information can be output on the GPIOs to wake-up and inform the host MCU on the 3DLF interfaces activity (e.g. LFRX receiving data, LFRX FIFO contains at least 1byte, f_{RCO} …). There is also the possibility, for the host MCU, to read-out the LFRX_STATES bits to be informed on the 3DLF interfaces activity.

The 3DLF state machine can operate in 3 different modes, selected by LF_MODE[1:0]:

1. Receive, constantly monitor the LF-interfaces for the presence of a valid telegram, wake-up the host MCU and decode the incoming LF data.
2. Transmit, to load-modulate information on the LF1 interface. This mode is used in battery-less mode to operate as a passive RFID transponder.
3. Measure RSSI, monitor the receive signal strength of the selected LF-interfaces.

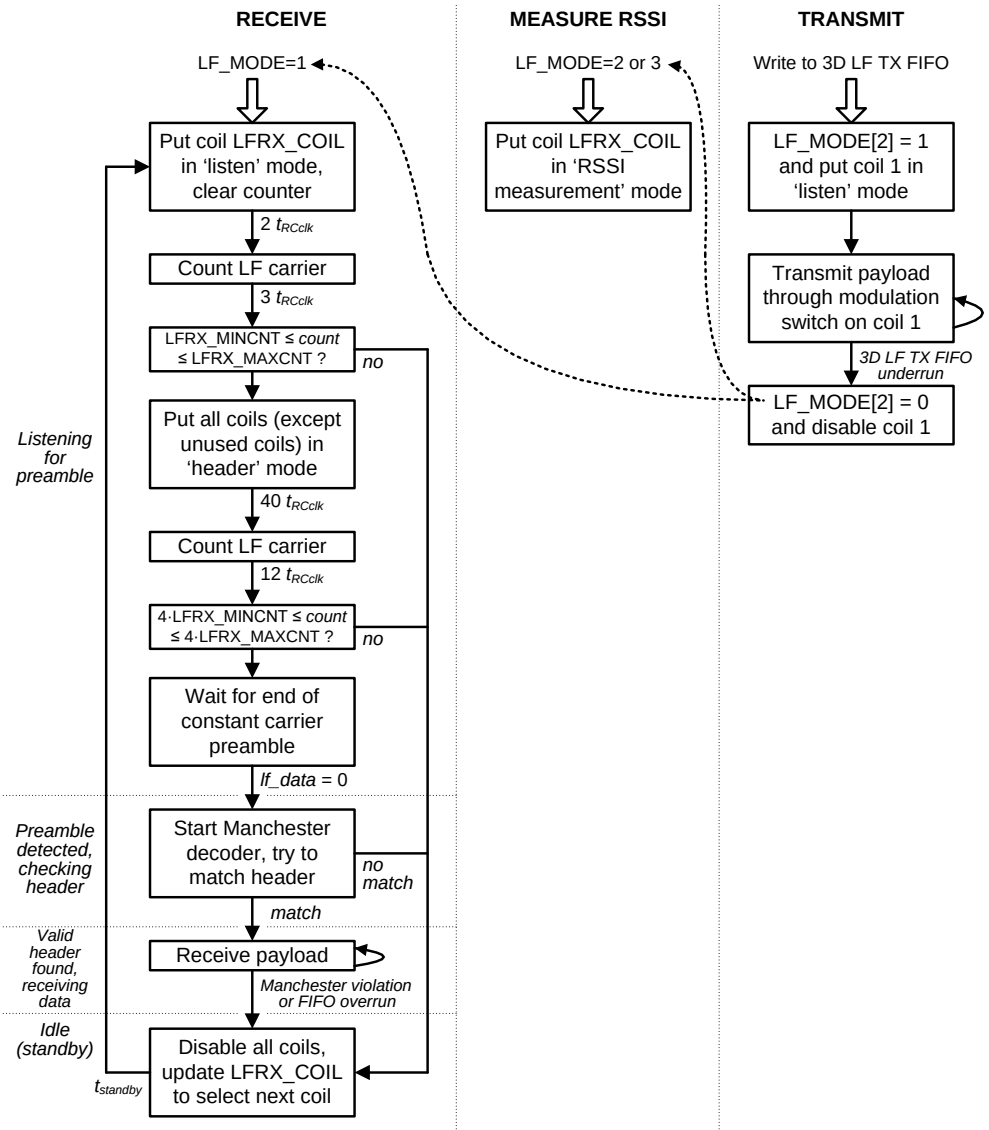


Figure 4: MLX73290-A 3DLF State-machine flow-chart

5.4.1 Reception mode (self-polling mode)

In reception mode, the 3DLF StateMachine (3DLF-SM) measures the frequency on the selected LF coil interface during a fix time of $5t_{RCO}$ (T_{LISTEN}). The measured frequency is compared to the min/max thresholds LFRX_MINCNT[4:0] and LFRX_MAXCNT[4:0] defined in bank 0. If the result is outside the range defined by these two thresholds, the 3DLF interface is going into low-power mode during a programmed time $T_{STANDBY}$ defined in LFRX_STBY[3:0] and then switch to the next LF coil interface. This scanning mechanism is continuously performed until a frequency measured within the min/max thresholds or an interruption is coming from the host MCU.

The selection of the LF-interface with which the scanning process is starting can be changed with the bits LFRX_COIL[1:0].

Once a valid frequency is measured, the 3DLF State Machine enables all coils and waits for a settling time of $40t_{RCO}$. At the end of this settling time, the coil with the strongest LF signal and the most reliable clock source is selected for a second measurement of the recovered LF carrier of $12t_{RCO}$.

If the measured LF is still within the min/max threshold values, the 3DLF-SM waits for the 1st falling edge of the header and starts the internal Manchester decoder to detect a valid header. As soon as detected, the 3DLF-SM stores all received Manchester data bits into the internal 8-Bytes FIFO buffer LFRX_FIFO[7:0], according to the data format described in the chapter below.

The reception stops upon the detection of a Manchester violation, FIFO overrun condition or if no valid preamble or header have been found. The 3DLF State Machine will automatically return in LF scanning activity.

The 3DLF self-polling mechanism is shown in the picture below:

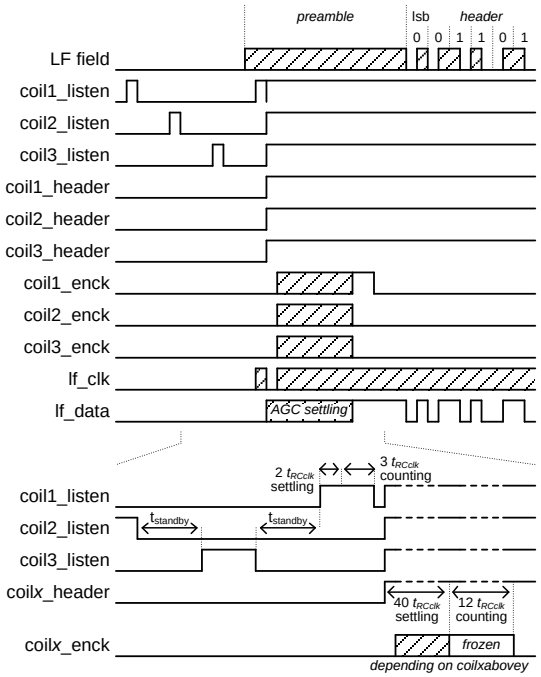


Figure 5: MLX73290-A 3DLF self-polling mechanism

5.4.2 Data format

Data (header + payload) should be modulated using OOK modulation. Manchester encoding with a data rate is fixed to 4kbps, corresponding to Manchester half symbol duration of 16 carrier periods. The Manchester decoder monitors the envelope signal and measures the time between edges in the envelope signal, to judge whether it corresponds to a short (0.5 symbol period), a long (1 symbol period) interval or to a violation (> 1 symbol period). The polarity can be configured using the bit LFRX_POL:

- Normal polarity (LFRX_POL to '0') : 0 = "01", 1 = "10"
- Reversed polarity (LFRX_POL to '1') : 0 = "10", 1 = "01"

5.4.3 Preamble definition

The preamble is a carrier burst that should be detected to prevent the chip from unintended wake-up in a noisy environment. To insure a correct wake-up, the minimum preamble should overlap one complete scanning window of $3 \cdot (T_{LISTEN} + T_{STANDBY})$ plus the settling time of $40t_{RCO}$, the measurement time of $12t_{RCO}$ and an additional time of $2t_{RCO}$.

$$T_{PREAMBLE} \geq 3 \cdot (T_{LISTEN} + T_{STANDBY}) + 54 \cdot t_{RCO} = 69 \cdot t_{RCO} + 3 \cdot T_{STANDBY}$$

5.4.4 Header definition

The header is a pre-defined symbol used by the 3DLF-SM to wake-up the host MCU and start decoding the payload. The header length can be programmed to 8, 16, or 32-bits with the bits LFRX_HDRLEN[2:0] and its value is defined in registers LFRX_HDR[31:0]. It is also possible to disable the header detection. In this case, the 3DLF-SM will not look for any header and will start to decode the payload directly after receiving the preamble.

Note: Care should be taken that the ***header is always configured LSB-first with a Manchester polarity to 0***, whatever the position of the bits LFRX_ORDER and LFRX_POL.

5.4.5 Min/Max Threshold definition

The min/max thresholds are defined in the bytes LFRX_MINCNT[4:0] and LFRX_MAXCNT[4:0], in Bank 0 (registers 0x50 and 0x51). The min/max thresholds can be defined with the following formula, the default values are set to 6_{10} and 25_{10}:

$$f_{MIN/MAX} = \frac{LFRX\_MIN(MAX)CNT[4:0] \pm 1}{3 \cdot f_{RCO}}$$

5.4.6 RSSI Mode

The MLX73290-A features a receive signal strength indicator (RSSI) block used to measure the level of the LF field. The RSSI measurement corresponds to the logarithmic functions of the RMS values measured on the LF-input selected with the bits LFRX_COIL[1:0] in the unbanked register 0x5B (could be the sum of all three).The minimum measured value is 1mVpp and the maximum is 1Vpp.

The 3DLF-SM is selected in RSSI mode with the bits LF_MODE[1:0] set to 1. In this mode, the internal AGC is switched OFF and the amplitude of the selected LF coil interface can be measured using the internal multi-purpose ADC with a resolution of 10bits. The LF coil interface to be measured can be selected with the bits LFRX_COIL[1:0] in the unbanked register 0x5B. By selecting these bits to 0, the RSSI information is the sum of the three LF interfaces.

Note: RSSI measurement must be done during a constant field carrier in order to get an accurate value.

5.4.7 Transmission Mode (TX)

In transmit mode, the MLX73290-A recovers the LF carrier frequency, to use it as a clock signal for the 3DLF State Machine, insuring that the device is always synchronized on the incoming LF field. The recovered LF clock is then divided by a programmable ratio between 1 to 128 (LFTX_RATE[7:0]) to obtain a *chip rate* between 1 to 125 kbps (by default 4kbps).

Data are back modulated on LF-input 1 (LF1), thanks to the internal switch opened/closed according to the transmitted data and polarity. Transmit data can come from the 8-bytes LFRX_FIFO[7:0] or directly from one GPIO pin according to the configuration of LFTX_MODE[2:0]. The polarity can also be selected with the bit LFTX_POL.

5.4.8 LF Backup Mode

The MLX73290-A integrates a bridge rectifier block, to recover the power from the LF-input 1 (LF1), to be stored on an external tank capacitor connected on the pin V_{field}.

If the battery voltage is below the minimum threshold of 2.1V, the internal power switch selects V_{field} as the most appropriate voltage source for the MLX73290-A (LF section only) and the host MCU (supplied through the output VMAIN clamped to max. 3.6V).

The flag BATTOK is reset to indicate to the host MCU that the MLX73290-A runs in low battery mode. The flag BATTOK is by default available on GPIO3.

5.4.9 LF FIFO

8-Bytes FIFO buffer is available in the MLX73290-A, to store data received from or to be transmitted to the 3DLF interface. FIFO buffer is accessible from register 0x5F LFRXFIFO[7:0].

Number of bytes available in the buffer can be read from registers 0x5D and 0x5E respectively, LFTXFIFO_CNT[3:0] and LFRXFIFO_CNT[3:0].

FIFO management information can be routed directly on the GPIOs or can be accessed by reading the level of the corresponding GPIO at the address 0x36 (unbanked register). For more information, please refer to the chapter 5.13 GPIO Pins.

5.5 RF Transceiver

The MLX73290-A is compliant with EN 300 220, FCC part 15, ARIB STD-67, the sub-GHz RF transceiver supports IEEE802.15.4 as well as proprietary OOK, (G)FSK-modulated communications in ISM bands between 300 and 960 MHz. Data rates between 0.15 and 250 kbps, FSK deviations of up to 125 kHz and RF output power levels between -20dBm and +13 dBm can be used.

The MLX73290-A embeds a 256-bytes FIFO to store/send the data to be received/sent during an RF transmission. This 256-bytes FIFO can be split into two buffers of 128-bytes each used independently for the transmission and/or the reception. This is performed with the bit FIFO_SIZE in unbanked register 0x27.

5.5.1 Frequency synthesizer

At the analog heart of the RF transceiver is a frequency synthesizer based on a Sigma-Delta fractional-N PLL. From a typical 32 MHz crystal reference clock, the PLL derives a quadrature LO-signal used for the mixers in the receive mode and to generate the carrier frequency in transmit mode. The PLL division ratio consists of a 6-bit integer part and a 19-bit fractional part, yielding to a resolution of 60 Hz. The VCO of the PLL requires to be calibrated; for this purpose a calibration algorithm is implemented in the digital domain of the MLX73290-A device.

5.5.2 Transmit mode (TX)

In RF transmit mode, the MLX73290-A outputs a CW signal on the differential RF outputs RFP and RFN. The output power can be configured from -20dBm up to 13dBm according to the bits RFTX_PWR[7:0] with the following tuning range (the simulated output powers are shown in the chapter 8.1 Simulated output power):

- bits [7:6] for selecting the output stages 1 to 4,
- bits [5:3] for selecting the octave range (octave 000 = power OFF, 111 = power saturation),
- bits [2:0] for linear power tuning.

The frequency of the CW can be adjusted with the bits CENTER_FREQ[24:0] according to the formula below.

For RF bands 0 or 1 (typ. 315 & 433MHz):

$$f_{RF} = \frac{f_{XTAL} \cdot CENTER\_FREQ[24:0]}{2^{20}}$$

For RF band 3 (typ. 868 & 915MHz):

$$f_{RF} = \frac{f_{XTAL} \cdot CENTER\_FREQ[24:0]}{2^{19}}$$

A packet handler reads data stored into the RFTX_FIFO to construct an RF packet including:

- Programmable preamble
- Synchronization word of 16, 24 or 32 bits
- Fixed or variable length payload (up to 255 bytes)
- Optional address byte
- Optional CRC-16 checksum.

The packet handler can be configured to adapt most of the used protocol formats. The bit order (LSB or MSB first) and bit polarity are configurable. After optional data whitening and Manchester encoding, the data stream of the RF packet enters the OOK or FSK modulator.

Note: D*ata whitening and Manchester encoding is only performed on the payload and not on the preamble and Sync Word.*

In case of OOK modulation, the PLL-based frequency synthesizer is programmed to the wanted carrier frequency and the power amplifier (PA) is switched ON and OFF.

In case of FSK modulation, the data stream is converted to a frequency deviation programmable between 0 and 125 kHz. The FSK signal directly modulates the PLL of the frequency synthesizer.

For both OOK and FSK modulation, the data stream can be selected with optional Gaussian pulse shaping EN_GAUSSIAN to reduce the spectral bandwidth of the transmitted RF signal.

5.5.3 Receive Mode (RX)

The receiver chain features an IQ receiver topology. The RF signal is converted to the low IF band by an image reject mixer (the IF is at 500kHz). In order to address a wide dynamic range, the LNA as well as the programmable gain amplifier (PGA) conditions the IF signal. An automatic gain control loop ensures a stable signal level at the input of the ADC which translates the signal to the digital domain. The baseband signal path features digital channel filtering, demodulation and extraction of clock and data. A de-serializer is used for extracting the payload from an incoming packet and writes the payload to a FIFO that can be read out by the SPI.

A packet handler scans the demodulated signal for a valid pattern followed by a programmable synchronization word of 16, 24 or 32 bits (SYNC_WORD[31:0] and SYNC_WORD_LEN[1:0]) and a fixed or variable length of payload (RFRX_FIFO of up to 255 bytes). An optional de-whitening operation as well as CRC-16 checksum verification could be enabled to reduce the load of the external host microcontroller.

5.5.3.1 Automatic Polling Mode

With the bits POLL_RFRX and EN_POLL, the MLX73290-A can be configured in automatic polling mode, using a programmable interval based on a 16-bit timer clocked with the internal calibrated RC oscillator (typ. At 15.6kHz), pre-scaled by a binary power of 2^{15} giving a maximum interval of 38 hours.

At the end of the waiting periods, the timer restarts and sets the corresponding IRQ flag TMR_FLAG, the MLX73290-A is set in receiver mode looking for a valid synchronization word SYNC_WORD[31:0], during a certain time as defined in the State Machine chapter just above. The RX period might be preceded by periodic recalibration as configured by CALIB_MODE. The RF state machine will eventually return to its stopped (idle) state after completion of the task (e.g. packet received) or when an error occurs (e.g. RX termination timer expires, PLL out of lock, FIFO overrun etc.). In the meantime, the polling timer continues to run, so the polling grid is in no way affected by how long it takes the RF transceiver to return to its idle state. This is important for RF protocols with beacons or timeslots at fixed intervals.

The following picture shows the basic functionality of the RF polling feature

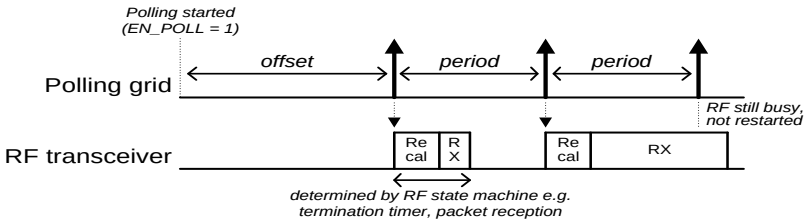


Figure 6: RF self-polling grid

The offset and polling period are configured with the registers POLL_EXP[4:0], POLL_OFFSET[15:0] and POLL_PERIOD[15:0] according to the following formulas:

$$Offset = \frac{2^{(11+POLL\_EXP)} \cdot (1 + POLL\_OFFSET)}{f_{XTAL}} [sec]$$

$$Period = \frac{2^{(11+POLL\_EXP)} \cdot (1 + POLL\_PERIOD)}{f_{XTAL}} [sec]$$

5.5.3.2 RSSI Information

RSSI information is available for the user in the register RSSI_HDR[6:0] which contains the RSSI information measured just after a valid header is detected.

5.5.4 State Machine

The RF State Machine supports a wide range of autonomous operations requiring little or no MCU overhead. To request a state change, the host MCU will write to the flag RF_MODE[2:0]:

- Calibrate TX/RX, then stop : to perform just a VCO calibration and nothing more
- Calibrate RX, then RX : to calibrate the VCO, then start reception
- RX waiting for header : to start reception, skipping the VCO calibration
- Calibrate TX, then TX : to calibrate the VCO, then start transmission
- TX transmitting payload : to start transmission, skipping the VCO calibration
- Stopped RX/TX : to abort any operation and return to the idle state

While writing to RF_MODE, the host MCU may also write a 0 to the RFTXFIFO_USE and RFRXFIFO_USE flags in the same register to clear the RF TX and/or RF RX FIFOs.

In receive mode, the MLX73290-A first waits for a matching synchronization word defined in registers SYNC_WORD[31:0], then move to the “RX receiving payload” state and start the reception of the payload. When the entire packet has been received, the RF_RXFLAG flag will be set, and the state machine will take the action selected by RXOK_ACT: it will stop, or resume RX after periodic recalibration as configured by CALIB_MODE. A packet handler scans the demodulated signal for a valid pattern followed by a programmable synchronization word of 16, 24 or 32 bits (SYNC_WORD[31:0] and SYNC_WORD_LEN[1:0]) and a fixed or variable length of payload (RFRX_FIFO of up to 255 bytes). An optional de-whitening operation as well as CRC-16 checksum verification could be enabled to reduce the load of the external host microcontroller.
Automatic Polling Mode

After successful reception, the MCU can read RSSI_HDR[6:0] and AFC_HDR[6:0] to obtain the RSSI and AFC values that have been measured during the reception of the packet (just after the SYNC_WORD). It may also read the TMR_HDR[15:0] to determine how much time has elapsed since the start of the received packet after the SYNC_WORD detection. This might be useful in slotted protocols, where the next transmission or reception should start at a certain distance relative to the beginning of the received packet.

If a CRC and/or address check is enabled, and the packet gets rejected on that basis, RXERR_ACT will determine whether the state machine will stop and report a CRC or address error, or flush the RF RX FIFO and resume the reception.

Furthermore there is the option to set a threshold RX_RSSI_TH on the RSSI, below which reception is inhibited. The MLX73290-A also features a termination timer programmable between 64µs and 32s (RXTERM_MANT[3:0] and RXTERM_EXP[3:0]). When the timer expires, termination may be postponed while RSSI is above the threshold, or while payload is being received, depending on the setting of the bit RXTERM_COND. Then the state machine will take the action selected by RXTERM_ACT: it will stop or recalibrate and resume reception.

When the PLL gets out of lock, depending on RXUNLOCK_ACT the state machine will stop and report a PLL out-of-lock error or it will take the same actions as for termination. When there is an overrun/underrun on the RFRXFIFO, the State Machine will stop and report a FIFO overrun/underrun error (RFRX_FIFO_USE) which can also be output on one GPIO.

Important Note: *The recommended setting of register RF_BIAS[7:0] in Bank 0 is 0x99. Smaller hex values can be selected for a lower receive current (at a reduced sensitivity). Yet the hex values should not be lower than 0x41 for the 433MHz and 0x5D for the 868MHz band.*

In transmit mode, after transmission of the payload, the State Machine will, depending on TXOK_ACT, stop, resume TX after periodic recalibration as configured by CALIB_MODE, or, after optional calibration, enter RX mode.

When DIRECT_MOD > 2 direct modulation is applied, with a fixed logic 0 or 1or with a level from one of the GPIO digital input pins. In this case the data-handler is bypassed and it is the responsibility of the microcontroller to terminate the transmission by changing RF_MODE. This mode will allow for the transmission of un-modulated as well as modulated carriers for characterization, test and type approval. A clock at the programmable symbol rate can be output on one of the GPIO pins for transmission of a synchronous bit stream.

When the PLL gets out-of-lock during transmission, the State Machine will always abort and report a PLL out of-lock error (PLL_LOCKED). When there is an overrun/underrun on the RFTXFIFO, the state machine will stop and report a FIFO overrun/underrun error (RFTX_FIFO_USE).

By putting KEEP_PLL_ON to ‘1’, the PLL can be kept running regardless the state of the RF transceiver, this is particularly useful for protocols where transmission or reception is triggered by an event and the normal startup delay of the PLL cannot be tolerated.

5.6 Modulation Settings

The below table provides an overview on the modulation settings. Continuous modulation can also be applied through the GPIOs. In this case the selected GPIO pin must be set as a digital input.

Modulation	mod_source	FSK/OOK	Manchester	Data-whitening	Comment
Continuous wave	Fixed logic 1	OOK	disable	disable	
Continuous modulation FSK Manchester	Fixed logic 1 or Fixed logic 0	FSK	enable	disable	
Continuous modulation FSK data whitening	Fixed logic 1 or Fixed logic 0	FSK	disable	enable	
Continuous modulation FSK GPIO	GPIO 0 GPIO 1 GPIO 2 GPIO 3	FSK	enable or disable	enable or disable	refer to sec 5.13 for GPIO input selection
Continuous modulation OOK Manchester	Fixed logic 1 or Fixed logic 0	OOK	enable	disable	
Continuous modulation OOK data whitening	Fixed logic 1 or Fixed logic 0	OOK	disable	enable	
Continuous modulation OOK GPIO	GPIO 0 GPIO 1 GPIO 2 GPIO 3	OOK	enable or disable	enable or disable	refer to sec 5.13 for GPIO input selection

Table 8 : Modulation Settings

5.7 Packet Handler

The MLX73290-A embeds a packet handler mechanism, able to manage the encoding/decoding of the transmit/received bytes contain in the RF FIFO. Different frame formats are supported and can be fully configured by the user, the following picture shows the different formats supported in transmit and receive modes:

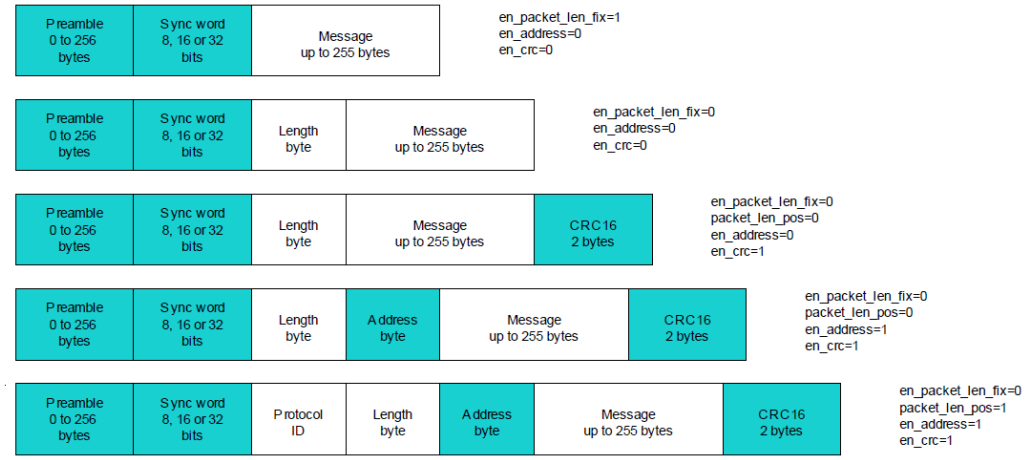


Figure 7: RF Packet Handler: supported frame formats

The packet handler is enabled by setting the bit en_packet to one, for the transmission mode. For the reception mode, the bit en_packet as well as the bit en_deserializer have both to be set to one. Both bits are available respectively in registers 0x18 and 0x27.

5.7.1.1 Preamble

A preamble can be automatically added to the packet structure. This feature can be turned on by simply setting the bit en_preamble signal to 1. The length of the preamble is given by the signal pattern_world_len[1:0] (number of times that the preamble byte is repeated) and the preamble itself is given by the preamble[7:0] in bank 0 (by default to 0x55).

5.7.1.2 Sync Word

The synchronization word is introduced automatically if the preamble is present. The length of the sync word is given by the sync_word_len. The synchronization word is always sent LSB first.

5.7.1.3 Packet Length

If the packet handler is enabled, it has to know the length of the packet that needs to be sent/received. This can be fixed or variable depending on the user settings. If the fixed solution is chosen, the en_packet_len_fix has to be set to 1. In this case the length of the packet in byte is given by the byte packet_len[7:0].

In the case of a variable packet length (en_packet_len_fix set to 0), the length is normally specified as one of the first bytes of the packet. The byte packet_len_pos[1:0] specifies the position of this byte (e.g. if set to 0, this means that the first byte sent/received defines the packet length).

The packet handler always considers the length of the packet from the first byte after the packet length byte until the last byte before the CRC. The bit packet_len_corr specifies the correction to apply to the packet length. This enables the user to provide/receive frame format with a length byte including itself and/or is included in the CRC computation.

The following picture shows the packet_len_corr principle.

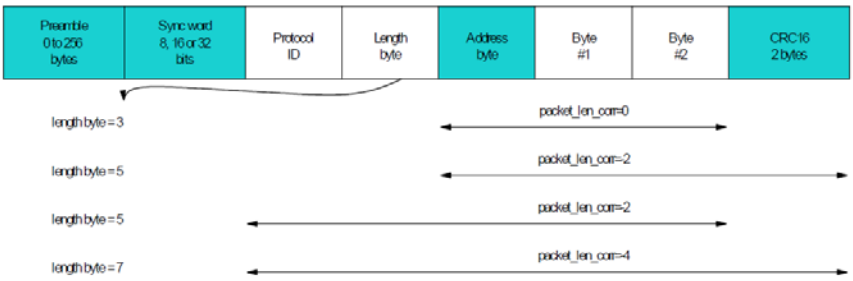


Figure 8: RF Packet Handler: Packet correction principle

5.7.1.4 Manchester Encoder/Decoder

A built-in Manchester encoder/decoder is implemented in the MLX73290-A, enabled with the bit EN_MANCHESTER in unbanked register 0x27. By default, the Manchester polarity is set to “normal” but it can also be reversed with the bit BIT_INVERT.

- Normal polarity (BIT_INVERT to ‘0’) : 0 = “01”, 1 = “10”
- Reversed polarity (BIT_INVERT to ‘1’) : 0 = “10”, 1 = “01”

The datastream to be filled in or taken from the RF FIFO is by default MSB-first. This can also be changed by the user in changing the bit LSB_FIRST.

Note: The Manchester encoding/decoding operation is only performed on the data to be sent (payload + address + CRC16) and NOT on the SYNC_WORD and PREAMBLE.

5.7.1.5 Address

An address can be inserted automatically after the packet length if the bit en_address is set to 1. The address is given by the byte address[7:0].

5.7.1.6 CRC16

A checksum CRC16 can be automatically computed and added/compared to the packet sent/received, by setting the bit en_crc to 1. In case of reception, the status bits rfrx_flag and rf_info[2:0] will be automatically updated in case of CRC error.

5.7.1.7 Multi-frame

If the en_multi_frame bit is set to 1, the multi-frame mode is enabled. A frame is composed by the data and the corresponding CRC. In this mode, a preamble and a single synchronization word are followed by multiple frames. As long as the en_multi_frame bit is set to 1, the packet handler continues to send/receive frames.

5.7.1.8 Data whitening

The packet handler also includes a data whitening process during the transmission or the reception of RF packets. In this case, all the data to be sent / received are encoded/decoded using a PN9 polynomial of X^9+X^5+1. The data whitening process is illustrated in the picture below. The data whitening process is enabled with the bit en_white.

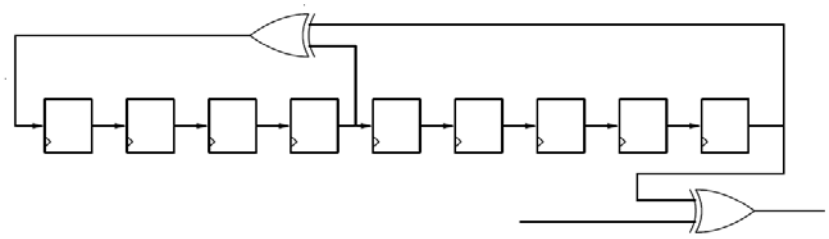


Figure 9: Frame data whitening PN9 polynomial structure

Note: The Data whitening operation is only performed on the data to be sent (payload + address + CRC16) and NOT on the SYNC_WORD and PREAMBLE.

5.8 Power Management Unit

The power management unit of the MLX73290-A performes the following operations:

- It measures the battery voltage (VDDA3) at power-on reset (POR) and decides whether the voltage is sufficient to power up the MLX73290-M and to supply the host MCU through pin VMAIN (if ≥ 2.1V).
- If the measured voltage at VDD3 is below the threshold level (VDDA3 < 2.1V), the pin VFIELD is used to supply the MLX73290-A and the host MCU.
- After power-up the internal power switch is locked to avoid switching back and forth between modes.
- When the IC is running, the power switch can still be controlled via SPI to select the supply source between VFIELD or VDDA3 (Register 0x0C of Bank0).
- The status of the power management state machine can be queried via SPI (Register 0x03 of Bank0).
- The voltage at VFIELD can be read via the general purpose ADC (see chapter 0).

Different monitoring blocks are used to report the status of the internal and external voltages, and to keep the digital control blocks in reset mode as long as the supply voltage has not reached a sufficient value:

Power-on reset (POR): This block is to maintain the digital circuitry in reset mode as long as the supply voltage is below a certain level at startup. When the supply voltage is sufficient, the reset mode is deactivated after a certain delay, which has to be sufficient to ensure correct internal state. While this is not a monitoring function per se, the state of the reset signal gives an indication as to when the supply voltage has reached the necessary level for the digital functionalities to work properly (meaning that the configuration registers are able to retain their state).

Brownout detector (BOD): Detects when the supply voltage drops below a certain threshold, even momentarily. The threshold should correspond to a voltage below which the digital functionalities cannot be guaranteed. The threshold crossing is detected without great precision but with a very low power consumption (less than 100nA). This monitoring block is mainly intended to be used for brownout detection when the overall power consumption is of key importance so that the bandgap voltage reference cannot be used.

Low battery detector (LBD): Uses the bandgap reference voltage to detect whether or not the external battery voltage is above or equal to its specified minimum level of 2.1V.

5.9 Programmable Timer / Clock Generator

A programmable timer / clock generator may periodically wake up the host MCU or it can provide a clock signal, derived from the RC oscillator, the calibrated RC clock or the crystal clock. A prescaler first divides the selected clock source by a programmable binary power between 1 and 231, and then by an 8-bit linear division ratio between 1 and 256.

The timer period is configured with the bits TMR_MANT[7:0] and TMR_EXP[4:0]. The following formula can be used to calculate the timer period, relative to the clock source selected by the bits TMR_SOURCE[1:0]:

$$TMR\_PERIOD = \frac{(TM\_MANT + 1) \cdot 2^{TMR\_EXP}}{f_{SOURCE}} \text{ [sec]}$$

The timer can be selected in timer or clock mode with the bit TMR_MODE. In timer mode, the timer stops when the flag gets set, and the MCU must clear the flag to restart the timer. In clock mode, the timer is continuously running thus providing a reference clock for the host MCU.

The timer is, by default configured to output the RC oscillator clock signal on GPIO2 without any division (i.e. ratio 1:1) so that it may act as a clock signal for the MCU. There is also the possibility to configure the timer output to another GPIO.

For more information about the programmable timer, please refer to the chapter 6.4 below.

5.10 System timer

The MLX73290-A embeds a 23-bit free-running counter that can serve as a time reference. When enabled, it increments at 7.8 kHz derived from the calibrated RC clock. Counter overflows (every ~18 minutes) will set a flag, which may wake-up the microcontroller. The firmware can then clear the flag and increment a counter in the microcontroller to extend the counter range to any length. To determine the elapsed time between two events, take a snapshot of this free-running system time at both moments and subtract these two values to find the elapsed time with 128 µs resolution.

For more information about the system timer, please refer to the chapter 6.4 Timers (0x40 to 0x4F).

5.11 General Purpose ADC

The external host MCU can use a built-in 10-bit general purpose ADC to measure several internal signals selected with the bits ADC_CH_SEL[3:0] (e.g. supply voltages, output of the RF power detectors, 3D LF field strength, temperature sensor, analog level of one of the GPIO pins). The ADC can be configured for continuous sampling or a single measurement (ADC_CONTINU bit set).

The conversion clock can be set to 1/16th, 1/32nd or 1/64th of the crystal clock ADC_CLK_SEL[1:0], corresponding to a period of conversion of respectively t_{AD} = 0.5, 1 or 2 µs with a 32MHz crystal. A full conversion cycle takes 128 clocks leading to a conversion time of 64, 128 or 256 µs, resulting in 16, 8 or 4 kS/s throughput.

The conversion is started with the bit ADC_START_EOC and the result stored into the register ADC_CAL[9:0]. Since the conversion results are 10 bit wide, the microcontroller will need to read them as 2 bytes through the SPI interface. This is an asynchronous process, so when the ADC operates in continuous sampling mode, the completion of a new conversion may coincide with the retrieval of the 2 bytes of the results of the previous conversion. Without special provisions the microcontroller may receive the first byte of the old conversion and the second byte of the new conversion, which could give a false reading. To prevent such inconsistencies, the generic ADC therefore takes a snapshot of the conversion results when the first byte is read, and returns the second part of the snapshot when the second byte is read in the same (burst mode) read access.

The generic ADC maintains a flag, ADC_NEWDATA, to indicate whether new results are available, primarily intended for continuous sampling mode. The completion of a conversion will set the flag, and reading the first byte of the results will clear the flag. The microcontroller may poll this flag to check if a new sample is available, and if so, it may continue reading the two byte result, which will clear the flag.

For more information about the general purpose ADC, please refer to the chapter 6.3 below.

5.12 SPI communication

The serial programming interface (SPI) is composed of three inputs and one output as shown in the following table.

SPI pin	I/O	Description
CS	input	SPI Chip Select active high
SDO	output	SPI Slave data output
SDI	input	SPI Slave data input
SCK	input	SPI Clock

The pin SDO is set to high impedance by the MLX73290-A when not transmitting SPI information; this allows a configuration using only one pin to successively send/receive information from/to the MLX73290-A. The two configurations using classical 4-pin and optimized 3-pin are illustrated below:

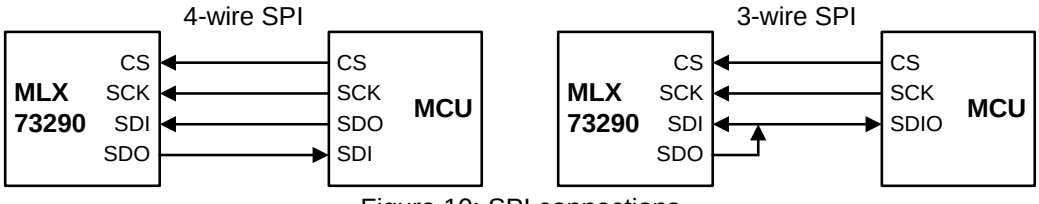


Figure 10: SPI connections

In read mode, the serial data changes on the falling edges of the serial clock and is latched, during write mode, on the rising clock edges. Data are transmitted MSB first.

Opposite to most conventional SPI devices, the CS chip select input of the MLX73290-A is active **high**. When the CS is set low, the MLX73290-A is deselected as SPI-slave; SCK and SDI can take any level, and SDO is tri-state. When CS goes high, the MLX73290-A becomes selected, and expects from the host MCU a 7-bit register address preceded by one bit of direction (**0 = write, 1 = read**).

A so-called burst mode is implemented in the MLX73290-A which automatically increments the address of the current register to be read/write. This operation is illustrated in the picture below:

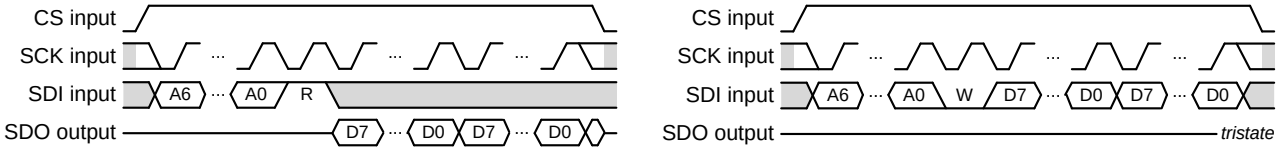


Figure 11: (burst) read/write SPI

The picture above is valid to address standard registers. To address the specific Bank0, the following procedure should be followed.

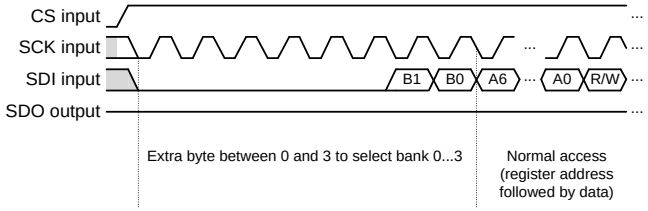


Figure 12: Specific access to Bank0 register

5.13 GPIO Pins

Four general purpose I/O (GPIO) pins are available in the MLX73290-A (GPIO0 to GPIO3). Several digital signals can be output, e.g. to be further used by the host MCU. Each GPIO pin has an 8-bit GPIO*x*_CH_SEL[7:0] (registers addresses 0x38 to 0x3B) setting that configures the I/O type of the corresponding pin (analog/digital, input/output) and the signal routing to/from the pin.

GPIO*x*_CH_SEL [7:0]	Signal	I/O type
x0000000	Disabled	Disabled
x0000001	GPIO*x*_Y with pull down	Digital input
x0000010	GPIO*x*_Y with pull up	Digital input
x0000011	GPIO*x*_Y	Digital input
x000010x : x0000110	*Reserved*	Disabled
x0000111	Internal analog line, pulled down	Analog I/O
x0001000 : x0001011	*Reserved*	Analog I/O
x0001100	Power Detector (PD)	Analog I/O
x0001101	*Reserved*	Analog I/O
x0001110	TEMPSENS	Analog I/O
0001xxxx 001xxxxx 01xxxxxx	See Table 10, signal level inverted when GPIO*x*_CH_SEL[0] = 1	Push-pull digital output
1001xxxx 101xxxxx 11xxxxxx	See Table 10, signal level inverted when GPIO*x*_CH_SEL[0] = 1	Open collector digital output

Table 9: Signal routed on GPIOs

The default values of GPIOs after power-on reset (POR) are:

- GPIO0 : READY
- GPIO1 : READY_NOT
- GPIO2 : TMR_FLAG
- GPIO3 : BATTOK

The digital signals are active high (unless otherwise specified). For GPIO*x* as digital output, the following truth table applies:

GPIOx_CH_SEL	Signal Name	Description
001000	Fixed logic 0	
001001	READY	MLX73290-A is ready after start-up sequence (POR)
001010	BATTOK	Battery level measured above the minimum level 2.1V.
001011	RCO	Output of uncalibrated internal RC oscillator
010100	*LOWBAT*	Output of low battery detector on VDDA3 /
010101	*XTAL_RDY*	Crystal clock is present and stable
011000	ADC_NEWDATA	New result from general purpose ADC available
011001	SYS_TIME_OVF	Internal system timer overflow
011010	TMR_FLAG	Programmable timer flag
011011	POLL_FLAG	RF Polling timer flag
011100	PLL_CYCLE_SLIP	A PLL cycle-slip has been registered since the last read from this register
011101	PLL_IN_LOCK	PLL successfully locked
011110	RFRX_CLK	RF clock output after datahandler
011111	RFRX_DATA	RF cata output after datahandler
100000	RFRX_WAIT_HDR	RF State Machine waiting for valid header
100001	RFRX_PAYLOAD	RF State Machine receiving the payload
100010	RFRX_WAIT_HDR_PAYLOAD	RF State Machine waiting for valid header or receiving payload
100011	RFTX_PAYLOAD	RF State Machine transmitting payload
100100	RF_STOPPED	RF State Machine stopped (RX or TX)
100101	RF_STOPPED_ERR	RF State Machine stopped with an error (RX or TX)
100110	RFTX_FIFO_OVRUDR	RF TX FIFO overrun/underrun error
100111	RFRX_FIFO_OVRUDR	RF RX FIFO overrun/underrun error
101000	RFRX_FIFO_1BYTE	RF RX FIFO contains at least 1byte
101001	RFRX_FIFO_64BYTES	RF RX FIFO contains at least 64bytes
101010	RFTX_FIFO_1BYTE	RF TX FIFO contains at least 1byte
101011	RFTX_FIFO_64BYTES	RF TX FIFO contains at least 64bytes
101100	RFTX_SYM_CLK	RF TX Manchester symbol clock
101101	RFRX_RSSI_ABOVE_THR	RX RSSI measured above threshold
101110	RFRX_PKT	RF datahandler packet received
101111	RFRX_PKT_3DLF_PAYLOAD	RF datahandler packet received or 3DLF receiving payload
110000	3DLF_TX_PAYLOAD	3DLF State Machine transmitting payload
110001	3DLF_RX_ PRB_HDR_DATA	3DLF State Machine checking preamble or header or receiving data

GPIOx_CH_SEL	Signal Name	Description
110010	3DLF_RX_DATA	3DLF State Machine receiving data
110011	3DLF_RX_HDR_DATA	3DLF State Machine checking header or receiving datas
110100	RFRX_PKT_3DLF_PAYLOAD_ SYSTIMEOVF	RF packet received or 3DLF receiving payload or system timer overflow
110101	3DLF_RX_1BYTE	3DLF RX FIFO contains at least 1byte
110110	3DLF_RX_4BYTES	3DLF RX FIFO contains at least 4bytes
110111	3DLF_RX_8BYTES	3DLF RX FIFO contains at least 8bytes
111000	RFRX_PKT_3DLF_PAYLOAD_ SYSTIMEOVF_TMRFLAG	RF packet received or 3DLF receiving payload or System timer overflow or Timer Flag
111001	3DLF_TX_1BYTE	3DLF TX FIFO contains at least 1byte
111010	3DLF_TX_4BYTES	3DLF TX FIFO contains at least 4bytes
111011	3DLF_TX_8BYTES	3DLF TX FIFO contains at least 8bytes
111100	3DLF_CLK_REC	3DLF RX recovered carrier clock signal
111101	3DLF_RX_DATA	3DLF RX envelop of decoded data
111110	3DLF_RX_SYM_CLK	3DLF Manchester symbol clock
111111	3DLF_RX_MAN_DATA	3DLF Manchester decoded data
Others	Melexis Reserved	

Table 10: GPIOs description

6 Register settings

The MLX73290-A is configured through a set of 126 unbanked registers for current use (addresses from 0x02 to 0x7F). One additional bank of 128 registers (Bank 0) is also available for specific information (addresses from 0x00 to 0x7F).

6.1 RF Transceiver (0x02 to 0x33)

Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RF Transceiver								
02	TMR_HDR[7:0]							
03	TMR_HDR[15:8]							
04		*Reserved*						
05		RSSI_HDR[6:0]						
06..09								
0A	DR_OFFSET[7:0]							
0B	LNA_12DB	LNA_ATTEN[1:0]		PGA_GAIN[4:0]				
0C		FILTER_GAIN_E[2:0]				FILTER_GAIN_M[2:0]		
0D	EN_CORRECT_ISI	EN_FINE_RECOV	EN_ROUGH_RECOV	EN_FAST_PRE_CR	DR_OFFS_ADJUST	AFC_MODE[1:0]		EN_CORRECT_CFREQ
0E..12								
13	RFTX_PWR[7:0]							
14	SYNC_WORD[7:0]							
15	SYNC_WORD [15:8]							
16	SYNC_WORD [23:16]							
17	SYNC_WORD [31:24]							
18	EN_D7M1	D7M1_TAG_NINT	EN_MULTI_FRAME	EN_DESERIAL	SYNC_WORD_LEN[1:0]		PATTERN_MAX_ERR[1:0]	
19	FIFO_SIZE	EN_PACKET_LEN_FIX	PACKET_LEN_POS[1:0]		PACKET_LEN_CORR[3:0]			
1A	PACKET_LEN[7:0]							
1B	ADDRESS[7:0]							
1C	CENTER_FREQ[2:0]							
1D	CENTER_FREQ[10:3]							
1E	CENTER_FREQ[18:11]							
1F			CENTER_FREQ[24:19]					
20			PWRDET_EN		RF_EN		BAND_SEL[1:0]	
21	DR_LIMIT[1:0]					DR_E[2:0]		
22			DR_M[5:0]					
23	MULT_EXP[3:0]				MULT_MANTISSA[3:0]			
24						TX_RAMP[2:0]		
25	PREAMBLE_LEN[7:0]							
26	IQ_CORR_EN	IQ_CORR_CAL	RF_RSSI_DEC[1:0]		RF_CHANBW[3:0]			
27	LSB_FIRST	BIT_	EN_MAN	EN_DATA	EN_	EN_	EN_CRC	EN_

		INVERT	CHESTER	WHITE	PREAMBLE	PACKET		ADDRESS
28	FSK_NOOK	EN_ GAUSSIAN	EN_INTERP	POSNEG_ MIX	POSNEG_IF	DIRECT_MOD[2:0]		
29					RX_RSSI_TH[3:0]			
2A	RXTERM_EXP[3:0]				RXTERM_MANT[3:0]			
2B	RXTERM_COND[1:0]					CALIB_MODE[2:0]		
2C				PWRUP_ MODE	PWRUP_TIME[3:0]			
2D	RXTERM _ACT		RXUNLOCK _ACT	RXERR _ACT	RXOK _ACT		TXOK_ACT[1:0]	
2E	RF_MODE[2:0]			POWER_MODE[2:0]			RFTXFIFO _USE	RFRXFIFO _USE
2Fr	RF_ RXFLAG	RF_MODE_SHORT[1:0]		RF_INFO[2:0]			RFTXFIFO _USE	RFRXFIFO _USE
2Fw	RF_MODE[2:0]						RFTXFIFO _USE	RFRXFIFO _USE
30	RFTXFIFO_CNT[7:0]							
31	RFRXFIFO_CNT[7:0]							
32r	RFRXFIFO[7:0]							
32w	RFTXFIFO[7:0]							
33	RANDOM[7:0]							

Table 11: Unbanked register map: RF Transceiver

Bit(s)	Signal	R/W	Init	Description
7…0	TMR_HDR[7:0]	R	-	Snapshot of the lower byte of the system time, taken after the detection of a valid header

Table 12: Unbanked register 0x02

Bit(s)	Signal	R/W	Init	Description
7…0	TMR_HDR[15:8]	R	-	Snapshot of the middle byte of the system time, taken after the detection of a valid header. To ensure consistency between the bytes, use one SPI access cycle to read both bytes of TMR_HDR

Table 13: Unbanked register 0x03

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	Not used, reads as 0
6…0	RSSI[6:0]	R	-	Current RSSI value, 1.5 dB increments

Table 14: Unbanked register 0x04

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	Not used, reads as 0
6…0	RSSI_HDR[6:0]	R	-	RSSI value frozen after header detection, 1.5 dB increments

Table 15: Unbanked register 0x05

Bit(s)	Signal	R/W	Init	Description

7...0	AFC[7:0]	RW	0	Lower byte of AFC value

Table 16: Unbanked register 0x06

Bit(s)	Signal	R/W	Init	Description
7...0	AFC[15:8]	RW	0	Upper byte of AFC value; to ensure consistency between the bytes, use one SPI access cycle to read both bytes of AFC.

Table 17: Unbanked register 0x07

Bit(s)	Signal	R/W	Init	Description
7...0	DR_OFFSET[7:0]	RW	0	Data rate offset in clock recovery

Table 18: Unbanked register 0x0A

Bit(s)	Signal	R/W	Init	Description
7	LNA_12DB	RW	0	Disable -12 dB attenuation in stage 1 of the LNAs
6...5	LNA_ATTEN[1:0]	RW	0	2-bit attenuation control in stage 2 of the LNAs : 0 = -18 dB 1 = -12 dB 2 = -6 dB 3 = 0 dB
4...0	PGA_GAIN[4:0]	RW	0	5 LSBs of 6-bit PGA gain setting, in 2 dB increments

Table 19: Unbanked register 0x0B

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	
6...4	FILTER_GAIN_E[2:0]	RW	0	Gain of the matched filter (exponent)
3	*Reserved*	R	0	
2...0	FILTER_GAIN_M[2:0]	RW	0	Gain of the matched filter (mantissa)

Table 20: Unbanked register 0x0C

Bit(s)	Signal	R/W	Init	Description
7	EN_CORRECT_ISI	RW	0	Enable the ISI (Inter-Symbol-Interference) correction
6	EN_FINE_RECOV	RW	0	Enables fine carrier recovery
5	EN_ROUGH_RECOV	RW	0	Enables rough carrier recovery
4	EN_FAST_PRE_CR	RW	0	Enables fast carrier recovery during the preamble
3	DR_OFFS_ADJUST	RW	0	Adjust data rate : 0 = no adjustment 1 = update DR_OFFSET at the end of the packet
2...1	AFC_MODE[1:0]	RW	0	AFC mode selection : 0 = no AFC 1 = AFC on the *fei_ok* signal 2 = AFC at the beginning of the payload 3 = AFC at the end of the packet
0	EN_CORRECT_ CFREQ	RW	0	Enable frequency correction

Table 21: Unbanked register 0x0D

Bit(s)	Signal	R/W	Init	Description
7...0	RFTX_PWR[7:0]	RW	0	Output power, see chapter 5.5.2 for details

Table 22: Unbanked register 0x13

Bit(s)	Signal	R/W	Init	Description
7...0	SYNC_WORD[7:0]	RW	0	First byte of synchronization word

Table 23: Unbanked register 0x14

Bit(s)	Signal	R/W	Init	Description
7...0	SYNC_WORD[[15:8]	RW	0	Second byte of synchronization word

Table 24: Unbanked register 0x15

Bit(s)	Signal	R/W	Init	Description
7...0	SYNC_WORD[[23:16]	RW	0	Third byte of synchronization word

Table 25: Unbanked register 0x16

Bit(s)	Signal	R/W	Init	Description
7...0	SYNC_WORD[[31:24]	RW	0	Fourth byte of synchronization word

Table 26: Unbanked register 0x17

Bit(s)	Signal	R/W	Init	Description
7	EN_D7M1	RW	0	Enable DASH7 mode 1
6	D7M1_TAG_NINT	RW	0	DASH7 mode 1 : 0 = interrogator 1 = tag
5	EN_MULTI_FRAME	RW	0	Enable the reception and transmission of packets consisting of multiple frames
4	EN_DESERIAL	RW	0	Enable data-handler in RF RX
3…2	SYNC_WORD_ LEN[1:0]	RW	0	Length of the synchronization word: 0 = 16 bits 1 = 24 bits 2 = 32 bits 3 = no synchronization pattern (only disables the pattern for RX, in TX the full 32-bit pattern will be transmitted)
1…0	SYNC_WORD_MAX_ERR [1:0]	RW	0	Maximum number of errors tolerated in received synchronization word

Table 27: Unbanked register 0x18

Bit(s)	Signal	R/W	Init	Description
7	FIFO_SIZE	RW	0	RF FIFO organization : 0 = single FIFO of 256 bytes 1 = two FIFOs of 128 bytes each
6	EN_PACKET_LEN_FIX	RW	0	Packet length : 0 = variable 1 = fixed
5…4	PACKET_LEN_POS [1:0]	RW	0	Position of the packet length byte, starting from the synchronization word (only applicable when the packet length is not fixed)
3…0	PACKET_LEN_CORR [3:0]	RW	0	Signed word that specifies how the packet length should be corrected

Table 28: Unbanked register 0x19

Bit(s)	Signal	R/W	Init	Description
7…0	PACKET_LEN[7:0]	RW	0	Fixed packet length mode: packet length in Byte Variable packet length mode: max. packet length in Byte

Table 29: Unbanked register 0x1A

Bit(s)	Signal	R/W	Init	Description
7…0	ADDRESS[7:0]	RW	0	Address to be transmitted or checked when address byte is enabled

Table 30: Unbanked register 0x1B

Bit(s)	Signal	R/W	Init	Description
7…5	CENTER_FREQ[2:0]	RW	0	Lower 3 bits of the fractional division ratio of the PLL for the center frequency
4…0	*Reserved*	R	0	Not used, reads as 0

Table 31: Unbanked register 0x1C

Bit(s)	Signal	R/W	Init	Description
7...0	CENTER_FREQ[10:3]	RW	0	Middle 8 bits of the fractional division ratio of the PLL for the center frequency

Table 32: Unbanked register 0x1D

Bit(s)	Signal	R/W	Init	Description
7...0	CENTER_FREQ[18:11]	RW	0	Upper 8 bits of the fractional division ratio of the PLL for the center frequency

Table 33: Unbanked register 0x1E

Bit(s)	Signal	R/W	Init	Description
7...6	*Reserved*	R	0	Not used, reads as 0
5...0	CENTER_FREQ[24:19]	RW	0	Upper 6 bits of the center frequency, corresponding to the integer division ratio of the PLL

Table 34: Unbanked register 0x1F

Bit(s)	Signal	R/W	Init	Description
7...5	*Reserved*	R	0	
4	PWRDET_EN	RW	0	Enable power detector PD if set
3	RF_EN	RW	0	Enable RF Front-end
2	Reserved	RW	0	
1...0	BAND_SEL[1:0]	RW	0	RF frequency band selection : 0 = 299 – 331 MHz frequency range 1 = 425 – 471 MHz frequency range 2 = 607 – 615 MHz frequency range 3 = 864 – 956 MHz frequency range

Table 35: Unbanked register 0x20

Bit(s)	Signal	R/W	Init	Description
7...6	DR_LIMIT[1:0]	RW	0	Limits of the data rate recovery : 0 = no data rate recovery 1 = ± 3.1% of the data rate 2 = ± 6.3% of the data rate 3 = ± 12.5% of the data rate
4...0	*Reserved*	R	0	
2...0	DR_E[2:0]	RW	0	Exponent to set the data rate

Table 36: Unbanked register 0x21

Bit(s)	Signal	R/W	Init	Description
7...6	*Reserved*	R	0	
5...0	DR_M[5:0]	RW	0	Mantissa to set the data rate

Table 37: Unbanked register 0x22

Bit(s)	Signal	R/W	Init	Description
7...4	MULT_EXP[3:0]	RW	0	Scaling to be applied to the pulse shaping coefficients by shifting them in the modulator, equivalent to 2^{MULT_EXP}
3...0	MULT_MANTISSA[3:0]	RW	0	Mantissa of the coefficient that multiplies the signal, equal to (16 + MULT_MANTISSA) / 16

Table 38: Unbanked register 0x23

Bit(s)	Signal	R/W	Init	Description
7...3	*Reserved*	R	0	Not used, reads as 0
2...0	TX_RAMP[2:0]	RW	0	TX ramp up/down duration: 0 = no ramp up/down 1 = 32 µs 2 = 16 µs 3 = 8 µs 4 = 192 µs 5 = 96 µs 6 = 48 µs 7 = 24 µs

Table 39: Unbanked register 0x24

Bit(s)	Signal	R/W	Init	Description
7...0	PREAMBLE_LEN[7:0]	RW	0	Length of the preamble to be transmitted

Table 40: Unbanked register 0x25

Bit(s)	Signal	R/W	Init	Description
7	IQ_CORR_EN	RW	0	Enable I/Q imbalance correction
6	IQ_CORR_CAL	RW	0	I/Q imbalance calibration in progress; set this bit to start I/Q imbalance calibration, automatically cleared by hardware when calibration is finished. Clear this bit to abort calibration. IQ_CORR_EN does not need to be set for the calibration.
5…4	RF_RSSI_DEC[1:0]	RW	0	Decay rate of RF RSSI : –1.5 dB at 0 = 1x symbol rate 1 = 2x symbol rate 2 = 4x symbol rate 3 = 8x symbol rate
3…0	RF_CHANBW[3:0]	RW	0	RF channel bandwidth : 0 = 600 kHz 1 = 300 kHz 2 = 200 kHz 3 = 150 kHz 4 = 120 kHz 5 = 100 kHz 6 = 75 kHz 7 = 60 kHz 8 = 50 kHz 9 = 38 kHz 10 = 30 kHz 11 = 25 kHz 12 = 19 kHz 13 = 15 kHz 14 = 13 kHz 15 = 9 kHz

Table 41: Unbanked register 0x26

Bit(s)	Signal	R/W	Init	Description
7	LSB_FIRST	RW	0	Select the bit order : 0 = MSB first 1 = LSB first
6	BIT_INVERT	RW	0	Invert the polarity of the data bits
5	EN_MANCHESTER	RW	0	Enable Manchester coding of the data bits
4	EN_DATAWHITE	RW	0	Enable data whitening
3	EN_PREAMBLE	RW	0	Enable transmission of a preamble
2	EN_PACKET	RW	0	Enable transmission and reception of packets
1	EN_CRC	RW	0	Add CRC to transmitted packets, check CRC of received packets
0	EN_ADDRESS	RW	0	Add address byte to transmitted packets, check address byte in received packets for match

Table 42: Unbanked register 0x27

Bit(s)	Signal	R/W	Init	Description
7	FSK_NOOK	RW	0	Select the modulation type : 0 = OOK 1 = FSK
6	EN_GAUSSIAN	RW	0	Enable Gaussian pulse shaping / matched filtering
5	EN_INTERP	RW	0	Enable interpolator on TX modulator output
4	POSNEG_MIX	RW	0	In RX, expect a positive or negative IF frequency in the down mixer
3	POSNEG_IF	RW	0	In RX, add or subtract the IF frequency to/from the center frequency (hi/lo-side injection)
2...0	DIRECT_MOD[2:0]	RW	0	Direct modulation source : 0, 1 = none, no direct modulation 2 = Fixed logic 0 3 = Fixed logic 1 4 = GPIO0 input 5 = GPIO1 input 6 = GPIO2 input 7 = GPIO3 input

Table 43: Unbanked register 0x28

Bit(s)	Signal	R/W	Init	Description
7...4	*Reserved*	R	0	Not used, reads as 0
3...0	RX_RSSI_TH[3:0]	RW	0	RSSI threshold value for carrier sense signal

Table 44: Unbanked register 0x29

Bit(s)	Signal	R/W	Init	Description
7...4	RXTERM_EXP[3:0]	RW	0	Exponent/Mantissa of RX termination timeout interval: 0 = $\frac{2048\cdot(1+RXTERM\_MANT)}{f_{xtalclk}}$
3...0	RXTERM_MANT[3:0]	RW	0	1...15 = $\frac{2048\cdot\left((RXTERM\_MANT+17)\cdot 2^{(RXTERM\_EXP-1)}\right)}{f_{xtalclk}}$

Table 45: Unbanked register 0x2A

Bit(s)	Signal	R/W	Init	Description
7…6	RXTERM_COND[1:0]	RW	0	After timeout has expired, postpone termination: 0 = always (i.e. never terminate) 1 = never (i.e. terminate unconditionally) 2 = as long as RSSI is above threshold, or payload is being received (after detection of a valid sync word) 3 = as long as a payload is being received
7…3	*Reserved*	R	0	
2…0	CALIB_MODE[2:0]	RW	0	Periodic (re)calibration mode: 0 = always recalibrate 1 = 1:4 2 = 1:8 3 = 1:16 4 = 1:32 5 = 1:64 6 = 1:128 7 = never recalibrate

Table 46: Unbanked register 0x2B

Bit(s)	Signal	R/W	Init	Description
7…5	*Reserved*	R	0	Not used, reads as 0
4	PWRUP_MODE	RW	0	Power-up sequence timing : 0 = Variable power-up time; the requested RF operation starts as soon as the power-up sequencing is completed 1 = Fixed power-up time; the requested RF operation starts after the timeout set by PWRUP_TIME[3:0], provided that the power-up sequence is completed
3…0	PWRUP_TIME[3:0]	RW	10	Timeout for power-up sequencing : 0 = 0.2 ms 1 = 0.25 ms 2 = 0.4 ms 3 = 0.5 ms 4 = 0.75 ms 5 = 1 ms 6 = 1.5 ms 7 = 2 ms 8 = 3 ms 9 = 4 ms 10 = 6 ms 11 = 8 ms 12 = 12 ms 13 = 16 ms 14 = 24 ms 15 = 32 ms When the timeout expires before the power-up sequence is completed, the pending RF mode (RX or TX) is aborted with an error

Table 47: Unbanked register 0x2C

Bit(s)	Signal	R/W	Init	Description
7	RXTERM_ACT	RW	0	Action to take for RX termination timeout 0 = go to error state 1 = flush RF RX FIFO, recalibrate RX, then RX
6	*Reserved*	R	0	Not used, reads as 0
5	RXUNLOCK_ACT	RW	0	Action to take when PLL gets out-of-lock in RX 0 = go to error state 1 = flush RF RX FIFO, recalibrate RX, then RX
4	RXERR_ACT	RW	0	Action to take when packet is received with incorrect length, address or CRC 0 = go to error state 1 = flush RF RX FIFO and restart RX
3	RXOK_ACT	RW	0	Action to take when packet received 0 = stop 1 = periodically (re)calibrate RX, then RX
2	*Reserved*	R	0	Not used, reads as 0
1...0	TXOK_ACT[1:0]	RW	0	Action to take upon TX completion 0 = stop 1 = periodically (re)calibrate TX, then TX 2 = RX 3 = calibrate RX, then RX

Table 48: Unbanked register 0x2D

Bit(s)	Signal	R/W	Init	Description
7...5	RF_MODE[2:0]	RW	0	Present RF mode: 0 = stopped TX 1 = stopped RX 2 = TX 3 = RX 4 = calibrate TX, then stop 5 = calibrate RX, then stop 6 = calibrate TX, then TX 7 = calibrate RX, then RX
4...2	POWER_MODE[2:0]	RW	3	Automatic power sequencer override: 0 = no override, VDIG, crystal oscillator and PLL OFF unless requested by internal functions, VDIG and crystal oscillator not kept ON when RF RX or TX FIFO not empty 1 = Force VDIG and crystal oscillator ON, POWER_MODE changes to 3 upon next write to RF TX FIFO 2 = keep VDIG ON when RF RX or TX FIFO not empty 3 = keep VDIG and crystal oscillator ON when RF RX or TX FIFO not empty 4 = Force VDIG ON 5 = Force VDIG ON, keep crystal oscillator ON when RF RX or TX FIFO not empty 6 = Force VDIG and crystal oscillator ON 7 = Force VDIG, crystal oscillator and PLL ON
1	RFTXFIFO_USE	RW	0	RF TX FIFO status: 0 = empty, overrun or underrun 1 = not empty (in use) Write 0 to flush RF TX FIFO, 1 to preserve FIFO contents
0	RFRXFIFO_USE	RW	0	RF RX FIFO status: 0 = empty, overrun or underrun 1 = not empty (in use) Write 0 to flush RF RX FIFO, 1 to preserve FIFO contents

Table 49: Unbanked register 0x2E

Bit(s)	Signal	R/W	Init	Description
7	RF_RXFLAG	R	0	Packet received, with correct length, address and CRC (if checking enabled); cleared when RF RX FIFO is flushed or a byte is read from the RF RX FIFO
6…5	RF_MODE_SHORT [1:0]	R	0	Present RF mode (read-only) : 0 = stopped TX 1 = stopped RX 2 = TX 3 = RX
4…2	RF_INFO[2:0]	R	0	Additional info on present RF mode, when RF_MODE = 0 or 1 (stopped RX / TX) : 0 = OK 1 = Power-up sequence timed out 2 = PLL out of lock 3 = FIFO error (over- or underrun) 4 = RX termination timer expired 5 = Invalid packet length received 6 = Incorrect address received 7 = Incorrect CRC received When RF_MODE = 2…7 (calibrate, RX or TX) : 0 = Powering up (LDOs, XTAL, PLL etc.) 1 = Calibrating VCO 2 = Waiting for PLL lock 3 = *Reserved* 4 = RX waiting for header 5 = RX receiving payload 6 = TX waiting for FIFO data 7 = TX transmitting payload
1	RFTXFIFO_USE	R	0	RF TX FIFO status: 0 = empty, overrun or underrun 1 = not empty (in use)
0	RFRXFIFO_USE	R	0	RF RX FIFO status: 0 = empty, overrun or underrun 1 = not empty (in use)

Table 50: Unbanked register 0x2F (***read***)

Bit(s)	Signal	R/W	Init	Description
7…5	RF_MODE[2:0]	W	0	Present RF mode: 0 = stopped TX 1 = stopped RX 2 = TX 3 = RX 4 = calibrate TX, then stop 5 = calibrate RX, then stop 6 = calibrate TX, then TX 7 = calibrate RX, then RX
4…2	*Reserved*	R	-	
1	RFTXFIFO_USE	W	0	Write 0 to flush RF TX FIFO, 1 to preserve FIFO contents
0	RFRXFIFO_USE	W	0	Write 0 to flush RF RX FIFO, 1 to preserve FIFO contents

Table 51: Unbanked register 0x2F (***write***)

Bit(s)	Signal	R/W	Init	Description
7...0	RFTXFIFO_CNT[7:0]	R	0	Number of bytes in the RF TX FIFO When the FIFO contains 256 bytes, RFTXFIFO_CNT will be 0 but RFTXFIFO_USE will be active. When RFTXFIFO_USE is 0, RFTXFIFO_CNT is normally 0 (FIFO empty) but can also indicate an underrun (count = 254) or overrun (count = 255)

Table 52: Unbanked register 0x30

Bit(s)	Signal	R/W	Init	Description
7...0	RFRXFIFO_CNT[7:0]	R	0	Number of bytes in the RF RX FIFO When the FIFO contains 256 bytes, RFRXFIFO_CNT will be 0 but RFRXFIFO_USE will be active. When RFRXFIFO_USE is 0, RFRXFIFO_CNT is normally 0 (FIFO empty) but can also indicate an underrun (count = 254) or overrun (count = 255)

Table 53: Unbanked register 0x31

Bit(s)	Signal	R/W	Init	Description
7...0	RFRXFIFO[7:0]	R	-	Accesses the data in the RF RX FIFO The register address is not auto-incremented

Table 54: Unbanked register 0x32 (***read***)

Bit(s)	Signal	R/W	Init	Description
7...0	RFTXFIFO[7:0]	W	-	Accesses the RF TX FIFO The register address is not auto-incremented

Table 55: Unbanked register 0x32 (***write***)

Bit(s)	Signal	R/W	Init	Description
7...0	RANDOM[7:0]	R	0	Random data, harvested noise of Sigma-Delta ADCs The register address is not auto-incremented

Table 56: Unbanked register 0x33

6.2 Status Byte & GPIOs (0x34 to 0x3B)

Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Status								
34								
35	BATTOK	PLL_ LOCKED	CYCLE_ SLIP	RSSI_ GOOD	FEI_OK			
GPIO multiplexing								
36					GPIO3	GPIO2	GPIO1	GPIO0
37	GPIO3_DRV[1:0]		GPIO2_DRV[1:0]		GPIO1_DRV[1:0]		GPIO0_DRV[1:0]	
38		GPIO0_CH_SEL[6:0]						
39		GPIO1_CH_SEL[6:0]						
3A		GPIO2_CH_SEL[6:0]						
3B		GPIO3_CH_SEL[6:0]						

Table 57: Unbanked register map: Status & GPIOs

Bit(s)	Signal	R/W	Init	Description
7	BATTOK	R	-	Started in : 0 = Battery backup mode 1 = Normal mode
6	PLL_LOCKED	R	-	PLL is currently in-lock
5	CYCLE_SLIP	RC	-	A PLL cycle-slip has been registered since the last read from this register (cleared by reading this register)
4	RSSI_GOOD	R	-	RSSI level above threshold (carrier sense)
3	FEI_OK	R	-	Frequency error indicator stable
2...0	*Reserved*	R	0	

Table 58: Unbanked register 0x35

Bit(s)	Signal	R/W	Init	Description
7...4	*Reserved*	R	0	Not used, reads as 0
3	GPIO3	R	-	Current level of GPIO3
2	GPIO2	R	-	Current level of GPIO2
1	GPIO1	R	-	Current level of GPIO1
0	GPIO0	R	-	Current level of GPIO0

Table 59: Unbanked register 0x36

Bit(s)	Signal	R/W	Init	Description
7...6	GPIO3_DRV[1:0]	RW	0	Sets the driving strength of GPIO3 when used as digital output: 0 = 3 mA 1 = 6 mA 2 = 9 mA 3 = 12 mA
5...4	GPIO2_DRV[1:0]	RW	0	Sets the driving strength of GPIO2 when used as digital output
3...2	GPIO1_DRV[1:0]	RW	0	Sets the driving strength of GPIO1 when used as digital output
1...0	GPIO0_DRV[1:0]	RW	0	Sets the driving strength of GPIO0 when used as digital output

Table 60: Unbanked register 0x37

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	
6...0	GPIO0_CH_SEL[6:0]	RW	0x12	See chapter 5.13

Table 61: Unbanked register 0x38

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	
6...0	GPIO1_CH_SEL[6:0]	RW	0x13	See chapter 5.13

Table 62: Unbanked register 0x39

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	
6...0	GPIO2_CH_SEL[6:0]	RW	0x34	See chapter 5.13

Table 63: Unbanked register 0x3A

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	
6...0	GPIO3_CH_SEL[6:0]	RW	0x14	See chapter 5.13

Table 64: Unbanked register 0x3B

6.3 General purpose ADC (0x3C to 0x3F)

Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
GPADC								
3C	ADC_REF_SEL[2:0]				ADC_CH_SEL[3:0]			
3D	ADC_ NEWDATA				ADC_ CONTINU	ADC_CLK_SEL[1:0]		ADC_START _EOC
3E	ADC_CAL[7:0]							
3F							ADC_CAL[9:8]	

Table 65: Unbanked register map: GPADC

Bit(s)	Signal	R/W	Init	Description
7...5	ADC_REF_SEL[2:0]	RW	0	Reference select for the generic ADC : 0 = bandgap voltage 1.2V 1 = VDDA3 2 = VDDA3 / 2 3 = VANA (1.7V nom) 4 = AIO0 5 = AIO1 6 = AIO2 7 = AIO3
4	*Reserved*	R	0	Not used, reads as 0
3...0	ADC_CH_SEL[3:0]	RW	0	Channel select for the generic ADC : 0 = 0.3 x VDDA3 1 = 0.3 x VMAIN 2 = 0.6 x VDIG 3 = 0.6 x VANA 4 = 0.6 x VVCO 5 = 0.6 x VPA 6 = *Reserved* 7 = Power Detector (PD) 8 = AIO0 9 = AIO1 10 = AIO2 11 = AIO3 12 = TEMPSENS 13 = 3D LF RSSI 14 = *Reserved* 15 = *Reserved*

Table 66: Unbanked register 0x3C

Bit(s)	Signal	R/W	Init	Description
7	ADC_NEWDATA	RW H/W set clear	0	New data sample available, can be cleared, not set. Set by hardware upon completion of an ADC measurement, automatically cleared by hardware when lower byte of conversion results is read.
6…4	*Reserved*	R	0	
3	ADC_CONTINU	RW	0	Generic ADC measurement mode : 0 = single measurement 1 = continuous measurement Write protected when ADC_START_EOC = 1
2…1	ADC_CLK_SEL[1:0]	RW	0	Clock select for the general purpose ADC: 0 = RC oscillator (500 µs/conversion typ.) 1 = XTAL / 64 (256 µs/conversion) 2 = XTAL / 32 (128 µs/conversion) 3 = XTAL / 16 (64 µs/conversion)
0	ADC_START_EOC	RW H/W clear	0	Enable general purpose ADC. Set this bit to start ADC measurements, clear this bit to stop / abort ADC measurements. Automatically cleared by hardware upon completion of an ADC measurement when ADC_CONTINU = 0 (single measurement mode), can be polled by host to wait for completion

Table 67: Unbanked register 0x3D

Bit(s)	Signal	R/W	Init	Description
7…0	ADC_CAL[7:0]	R	-	Lower byte of 10-bit conversion result of the generic ADC

Table 68: Unbanked register 0x3E

Bit(s)	Signal	R/W	Init	Description
7…2	*Reserved*	R	0	
1…0	ADC_CAL[9:8]	R	-	Upper bits of 10-bit conversion result of the generic ADC; to ensure consistency between the bytes, use one SPI access cycle to read both bytes of ADC_CAL

Table 69: Unbanked register 0x3F

6.4 Timers (0x40 to 0x4F)

Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Timers								
40	TMR_MANT[7:0]							
41	TMR_SOURCE[1:0]		TMR_MODE	TMR_EXP[4:0]				
42	TMR_FLAG							
43								
44	SYS_TIME[7:0]							
45	SYS_TIME[15:8]							
46	SYS_TIME_OVF	SYS_TIME[22:16]						
47	SYS_TIME_EN							
48	POLL_OFFSET[7:0]							
49	POLL_OFFSET[15:8]							
4A	POLL_PERIOD[7:0]							
4B	POLL_PERIOD[15:8]							
4C	EN_POLL	POLL_FLAG	POLL_RFRX		POLL_EXP[3:0]			
4D								
4E	RC_CAL[7:0]							
4F						RC_CAL[10:8]		

Table 70: Unbanked register map: Timers

Bit(s)	Signal	R/W	Init	Description
7...0	TMR_MANT[7:0]	RW	0	8-bit period of programmable timer / clock generator; changes are glitch-free in clock generator mode Period = (TMR_MANT+1)·2^{TMR_EXP} clocks

Table 71: Unbanked register 0x40 (programmable timer)

Bit(s)	Signal	R/W	Init	Description
7...6	TMR_SOURCE[1:0]	RW	2	Clock source selector for programmable timer / clock generator : 0 = OFF, timer stopped and reset 1 = 32 MHz (typ.) crystal clock 2 = 32 kHz (typ.) RC oscillator 3 = 15.6 kHz (typ.) calibrated RC clock Changes are glitch-free in clock generator mode
5	TMR_MODE	RW	0	Mode of programmable timer / clock generator : 0 = Clock generator 1 = Timer
4...0	TMR_EXP[4:0]	RW	0	5-bit prescaler ratio of programmable timer / clock generator; changes are glitch-free in clock generator mode

Table 72: Unbanked register 0x41 (programmable timer)

Bit(s)	Signal	R/W	Init	Description
7	TMR_FLAG	RW	-	Output of programmable timer / clock generator IRQ flag in timer mode, that will stop the timer and needs to be cleared by the microcontroller
6...0	Reserved	R	0	Not used, reads as 0

Table 73: Unbanked register 0x42 (programmable timer)

Bit(s)	Signal	R/W	Init	Description
7...0	SYS_TIME[7:0]	RC	0	Lower byte of 23-bit free-running system time Any write to this register will reset the entire system time including the overflow flag

Table 74: Unbanked register 0x44 (system timer)

Bit(s)	Signal	R/W	Init	Description
7...0	SYS_TIME[15:8]	RC	0	Middle byte of 23-bit free-running system time To ensure consistency between the bytes, use one SPI access cycle to read the lower, middle and upper byte of the system time

Table 75: Unbanked register 0x45 (system timer)

Bit(s)	Signal	R/W	Init	Description
7	SYS_TIME_OVF	RC	0	Overflow of the free-running system time, can be cleared by setting this bit to 0 through SPI
6...0	SYS_TIME[22:16]	RC	0	Upper byte of 23-bit free-running system time To ensure consistency between the bytes, use one SPI access cycle to read the lower, middle and upper byte of the system time

Table 76: Unbanked register 0x46 (system timer)

Bit(s)	Signal	R/W	Init	Description
7	SYS_TIME_EN	RW	0	Enable free-running system time Disabling the system time will pause the system time, but not clear it
6...0	Reserved	R	0	

Table 77: Unbanked register 0x47 (system timer)

Bit(s)	Signal	R/W	Init	Description
7...0	POLL_OFFSET[7:0]	RW	0	Lower byte of 16-bit offset of RF polling timer

Table 78: Unbanked register 0x48 (RF polling timer)

Bit(s)	Signal	R/W	Init	Description
7...0	POLL_OFFSET[15:8]	RW	0	Upper byte of 16-bit offset of RF polling timer Offset = $\frac{2^{(11+POLL\_EXP)} \cdot (1+POLL\_OFFSET)}{f_{xtalclk}}$ sec

Table 79: Unbanked register 0x49 (RF polling timer)

Bit(s)	Signal	R/W	Init	Description
7...0	POLL_PERIOD[7:0]	RW	0	Lower byte of 16-bit period of RF polling timer

Table 80: Unbanked register 0x49 (RF polling timer)

Bit(s)	Signal	R/W	Init	Description
7...0	POLL_PERIOD[15:8]	RW	0	Upper byte of 16-bit period of RF polling timer Period = $\frac{2^{(11+POLL\_EXP)} \cdot (1+POLL\_PERIOD)}{f_{xtalclk}}$ sec

Table 81: Unbanked register 0x4B (RF polling timer)

Bit(s)	Signal	R/W	Init	Description
7	EN_POLL	RW	0	Enable RF polling timer
6	POLL_FLAG	RW	0	IRQ flag of RF polling timer, set when timer expires
5	POLL_RFRX	RW	0	Enable RF RX polling
4	*Reserved*	R	0	
3...0	POLL_EXP[3:0]	RW	0	4-bit prescaler ratio of RF polling timer

Table 82: Unbanked register 0x4C (RF polling timer)

Bit(s)	Signal	R/W	Init	Description
7...0	RC_CAL[7:0]	RW	0xE8	Lower byte of calibration value for RC oscillator = $f_{xtalclk}$ / f_{RCclk}

Table 83: Unbanked register 0x4E (RCO calibration)

Bit(s)	Signal	R/W	Init	Description
7...3	*Reserved*	R	0	
2...0	RC_CAL[10:8]	RW	3	Upper bits of calibration value for RC oscillator. To ensure consistency between the bytes, use one SPI access cycle to read both bytes of RC_CAL. Write protected when calibrated RC clock is in use by one or more functions

Table 84: Unbanked register 0x4F (RCO calibration)

6.5 3DLF Transceiver (0x50 to 0x5F)

Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3D LF transceiver								
50			COIL1_TRIM[5:0]					
51			COIL2_TRIM[5:0]					
52			COIL3_TRIM[5:0]					
53			EN_3DLF	COIL_ENCK[1:0]		MOD_3DLF	COIL_ HEADER	COIL_ LISTEN
54	LFRX_HDR[7:0]							
55	LFRX_HDR[15:8]							
56	LFRX_HDR[23:16]							
57	LFRX_HDR[31:24]							
58								
59	LFRX_POL	LFRX_HDRLEN[2:0]			LFTX_POL	LFTX_MODE[2:0]		
5A	LFRX_MASK[2:0]			LFRX_ ORDER	LFRX_STBY[3:0]			
5B		LF_MODE[2:0]			LFRX_STATE[1:0]		LFRX_COIL[1:0]	
5C								
5D					LFTXFIFO_CNT[3:0]			
5E					LFRXFIFO_CNT[3:0]			
5Fr	LFRXFIFO[7:0]							
5Fw	LFTXFIFO[7:0]							

Table 85: Unbanked register map : 3DLF Transceiver

Bit(s)	Signal	R/W	Init	Description
7...6	*Reserved*	R	0	
5...0	COIL1_TRIM[5:0]	RW	0	6-bit capacitor tuning on 3DLF coil 1, 1.5pF per step

Table 86: Unbanked register 0x50

Bit(s)	Signal	R/W	Init	Description
7...6	*Reserved*	R	0	
5...0	COIL2_TRIM[5:0]	RW	0	6-bit capacitor tuning on 3DLF coil 2, 1.5pF per step

Table 87: Unbanked register 0x51

Bit(s)	Signal	R/W	Init	Description
7...6	*Reserved*	R	0	
5...0	COIL3_TRIM[5:0]	RW	0	6-bit capacitor tuning on 3DLF coil 3, 1.5pF per step

Table 88: Unbanked register 0x52

Bit(s)	Signal	R/W	Init	Description
7…6	*Reserved*	R	0	
5	EN_3DLF	RW	0	Force 3DLF front-end enabled, set to '0' for normal operation
4…3	COIL_ENCK[1:0]	RW	0	Recovered carrier clock source, set to '0' for normal operation : 0 = automatically selected 1 = Coil 1 2 = Coil 2 3 = Coil 3
2	MOD_3DLF	RW	0	Forces 3DLF TX modulation switch to close, set to '0' for normal operation
1	COIL_HEADER	RW	0	Forces masked coil(s) in header detection mode, set to '0' for normal operation
0	COIL_LISTEN	RW	0	Forces selected coil(s) in preamble detection mode, set to '0' for normal operation

Table 89: Unbanked register 0x53

Bit(s)	Signal	R/W	Init	Description
7…0	LFRX_HDR[7:0]	RW	0	3DLF header to be recognized in RX

Table 90: Unbanked register 0x54

Bit(s)	Signal	R/W	Init	Description
7…0	LFRX_HDR[15:8]	RW	0	3DLF header to be recognized in RX

Table 91: Unbanked register 0x55

Bit(s)	Signal	R/W	Init	Description
7…0	LFRX_HDR[23:16]	RW	0	3DLF header to be recognized in RX

Table 92: Unbanked register 0x56

Bit(s)	Signal	R/W	Init	Description
7…0	LFRX_HDR[31:24]	RW	0	3DLF header to be recognized in RX

Table 93: Unbanked register 0x57

Bit(s)	Signal	R/W	Init	Description
7	LFRX_POL	RW	0	3DLF RX polarity: 0 = Normal, Manchester pattern 01 will yield 0 as data bit 1 = Reverse, Manchester pattern 01 will yield 0 as data bit
6…4	LFRX_HDRLEN[2:0]	RW	0	3DLF header length: 0-3 = no header, start data reception after preamble 4 = 8-bit header (LFRX_HDR[7:0]) 5 = 16-bit header (LFRX_HDR[15:0]) 6 = *Reserved* 7 = 32-bit header(LFRX_HDR[31:0]) *Note: the header is always LSB first and Manchester encoded 01 = data 0, 10 = data 1, independent of the LFRX_ORDER and LFRX_POL settings*
3	LFTX_POL	RW	0	3DLF TX polarity: 0 = Normal, switch closed when NRZ bit from FIFO or GPIOx is 1 or during 1st chip of Manchester 1, 2nd chip of Manchester 0 1 = Reverse, switch closed when NRZ bit from FIFO or GPIOx is 0 or during 2nd chip of Manchester 1, 1st chip of Manchester 0
2…0	LFTX_MODE[2:0]	RW	0	3D LF TX modulation mode: 0 = NRZ modulation from FIFO, LSB first 1 = NRZ modulation from FIFO, MSB first 2 = Manchester modulation from FIFO, LSB first 3 = Manchester modulation from FIFO, MSB first 4 = direct modulation through GPIO0 5 = direct modulation through GPIO1 6 = direct modulation through GPIO2 = direct modulation through GPIO3 *Note: Only modes 0 to 3 require the 3DLF to be in active TX mode, the direct modulation modes are independent of the 3DLF state machine.*

Table 94: Unbanked register 0x59

Bit(s)	Signal	R/W	Init	Description
7…5	LFRX_MASK[2:0]	RW	0	Must be set to '111'
4	LFRX_ORDER	RW	0	Bit order in reception mode: 0 = LSB first 1 = MSB first
3…0	LFRX_STBY[3:0]	RW	0	See Table 6: LF characteristics

Table 95: Unbanked register 0x5A (3DLF state-machine)

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	
6…4	LF_MODE[2:0]	RW	0	3DLF state machine operating mode: 0 = OFF 1 = LF RSSI measurement (use GPADC to read-out RSSI value) 2, 3 = RX, scan polling enable 4 = TX, then switch OFF 5 = TX, then LF RSSI measurement (use GPADC to read-out RSSI value) 6, 7 = TX, then resume RX *Note: TX mode (LF_MODE[2] = 1) is automatically entered when the 3DLF TX FIFO is written and cannot be entered by writing a value ≥ 4 to LF_MODE. It can be prematurely aborted by writing a value < 4 to LF_MODE, this will also clear the 3DLF TX FIFO.*
3…2	LFRX_STATE[1:0]	R	0	Present 3D LF state: 0 = Idle (standby) 1 = Listening for preamble 2 = Preamble detected, checking header 3 = Valid header found, receiving data
1…0	LFRX_COIL[1:0]	RW	1	Selected coil: 0 = *Reserved* (in fact enables all used coils) 1 = Coil 1 2 = Coil 2 3 = Coil 3 Write protected when LF_MODE[1:0] > 0

Table 96: Unbanked register 0x5B (3DLF state-machine)

Bit(s)	Signal	R/W	Init	Description
7…4	*Reserved*	R	0	
3…0	LFTXFIFO_CNT[3:0]	R	0	Number of bytes (0…8) in the 3DLF TX FIFO Whenever LFTXFIFO_CNT > 0, the 3DLF is in TX mode

Table 97: Unbanked register 0x5D (3DLF FIFO)

Bit(s)	Signal	R/W	Init	Description
7…4	*Reserved*	R	0	
3…0	LFRXFIFO_CNT[3:0]	R	0	Number of bytes (0…8) in the 3D LF RX FIFO The 3DLF RX FIFO is automatically flushed when active reception starts upon detection of a valid header

Table 98: Unbanked register 0x5E (3DLF FIFO)

Bit(s)	Signal	R/W	Init	Description
7…0	LFRXFIFO[7:0]	R	0	Accesses the data in the 3DLF RX FIFO The register address is not auto-incremented

Table 99: Unbanked register 0x5F read (3DLF FIFO)

Bit(s)	Signal	R/W	Init	Description
7…0	LFTXFIFO[7:0]	W	0	Accesses the 3DLF TX FIFO The register address is not auto-incremented

Table 100: Unbanked register 0x5F write (3DLF FIFO)

6.6 Chip ID and soft Reset (register 0x7F)

Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Chip ID and soft reset								
7Fr	CHIP_ID							
7Fw	SOFTRESET							

Table 101: Unbanked register 0x7F

Bit(s)	Signal	R/W	Init	Description
7…0	CHIP_ID	R	0x11	Chip identification number

Table 102: Unbanked register 0x7F read

Bit(s)	Signal	R/W	Init	Description
7…0	SOFTRESET	W	-	Write 0x56 to trigger a soft reset of the chip.

Table 103: Unbanked register 0x7F write

6.7 Bank 0

Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Test and spare signals								
00..06								
07				PN9_ REVERSE	CRC_ RST_MODE	PN9_ MODE	PGA_ GAIN[5]	ADC_TEST
08-3B								
3C	RF_BIAS[7:0]							
3D..48								
49	PREAMBLE[7:0]							
4A..4F								
50				LFRX_MINCNT[4:0]				
51				LFRX_MAXCNT[4:0]				
52		LFRX_RATE[6:0]						
53	LFTX_RATE[7:0]							
54..7F								

Table 104: Bank0 register map

Bit(s)	Signal	R/W	Init	Description
7...5	*Reserved*	R	0	Not used, reads as 0
4	PN9_REVERSE	RW	1	Generate PN9 sequence : 0 = LSB first 1 = MSB first
3	CRC_RST_MODE	RW	0	Initialize CRC to : 0 = 0x0000 1 = 0xFFFF
2	PN9_MODE	RW	1	Perform PN9 sequence with reversed byte.
1..0	*Reserved*	R	0	

Table 105: Bank0 register 0x07

Bit(s)	Signal	R/W	Init	Description
7...0	RF_BIAS[7:0]	RW	0	Enable the RF RX functionality, has to be set to the following values depending on the frequency band selected: 315MHz = 0x99 433MHz = 0x99 868MHz and 915MHz = 0x99

Table 106: Bank0 register 0x3C

Bit(s)	Signal	R/W	Init	Description
7...0	PREAMBLE[7:0]	RW	0x55	Preamble pattern to be repeated according to PREAMBLE_LEN[7:0] in unbanked register 0x25

Table 107: Bank0 register 0x49

Bit(s)	Signal	R/W	Init	Description
7...5	*Reserved*	R	0	
4...0	LFRX_MINCNT[4:0]	RW	6	Minimum counter value for valid preamble, recommended setting = $3\frac{f_{LFcarrier,min}}{f_{RCclk,max}}$ – margin

Table 108: Bank0 register 0x50

Bit(s)	Signal	R/W	Init	Description
7...5	*Reserved*	R	0	
4...0	LFRX_MAXCNT[4:0]	RW	25	Maximum counter value for valid preamble, recommended setting = $3\frac{f_{LFcarrier,max}}{f_{RCclk,min}}$ – margin

Table 109: Bank0 register 0x51

Bit(s)	Signal	R/W	Init	Description
7	*Reserved*	R	0	
6...0	LFRX_RATE[6:0]	RW	18	Threshold value for Manchester decoding, recommended setting = $\frac{18}{32} \cdot \frac{f_{LFcarrier}}{f_{datarate}} = 18\ (for\ 4kbps)$

Table 110: Bank0 register 0x52

Bit(s)	Signal	R/W	Init	Description
7...0	LFTX_RATE[7:0]	RW	31	Ratio between LF carrier clock and TX chip rate chip rate = $2 \cdot \frac{f_{LFcarrier}}{LFTX\_RATE+1}$ When LFTX_RATE is even, every odd chip will have one carrier clock cycle extra LFTX_RATE = 0 is not supported, and will yield the chip rate of LFTX_RATE = 1

Table 111: Bank0 register 0x53

7 Application Information

7.1 Typical application schematic

The following schematic shows the typical application schematic using both LF and RF interfaces and gives an idea of the final external components count.

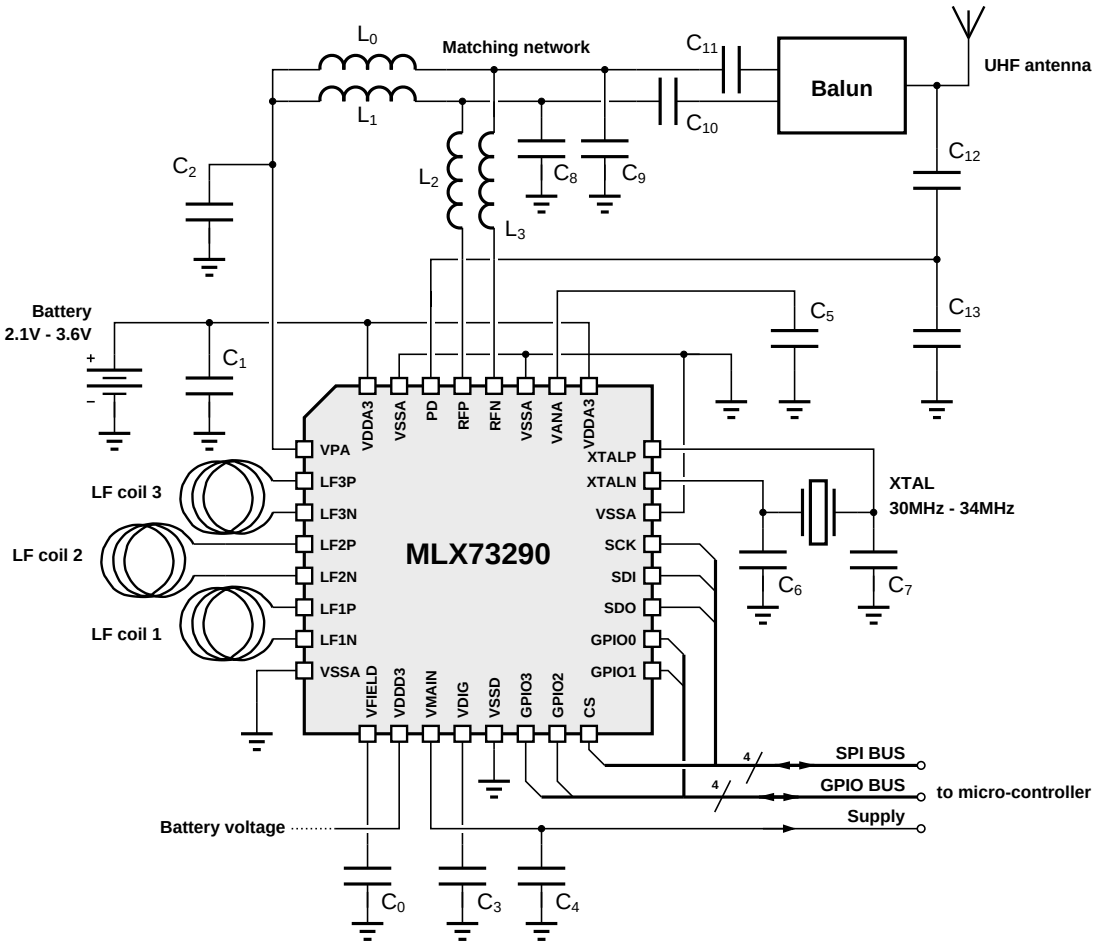


Figure 13 : Typical application schematic

7.1.1 TX/RX Combining Network

The RF ports of the MLX73290-A have been designed in order to achieve optimum performance in both TX and RX mode as well as for different RF power levels and at various frequency bands. For this purpose two inductors are used per single-ended RF port. Pin VPA provides a supply voltage that connects to the two inductors of the TX/RX combining network. In TX mode, this pin is internally switched to positive level, supplying the internal cascoded power amplifier (PA). In RX mode, pin VPA is internally connected to ground. **As a result the RF port impedance in RX mode matches the impedance in TX mode, yielding a power match in RX mode.**

7.1.2 Balun

A Balun is used to convert from differential input/output of the MLX73290-A to single-ended signal from/to the RF antenna. Off-the-shelf baluns are available on the market, depending on the wanted frequency range, the actual implementation will vary. Some SAW filters can also fulfil a balun functionality, which may be an interesting solution if it is necessary to filter out harmonics to comply with regulatory requirements. The easiest solution is to realize a lumped balun with discrete external components and integrated it within the RF matching network. A simple balun topology is illustrated below.

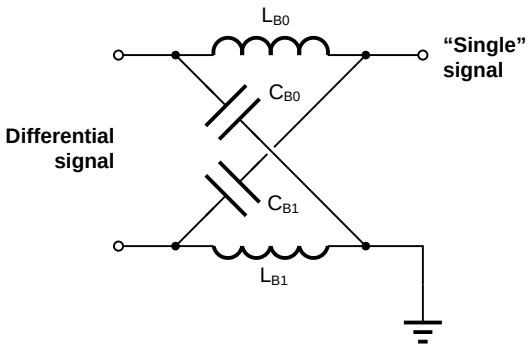


Figure 14: Balun made with discrete parts

7.1.3 External power switch usage

In the special case where the micro-controller does not have a low power standby mode (as would be for example the case with some dedicated secure core), the overall power consumption can be reduced by using the integrated polling mechanism and using an external power switch, e.g. a power MOSFET, as illustrated by Figure 15.

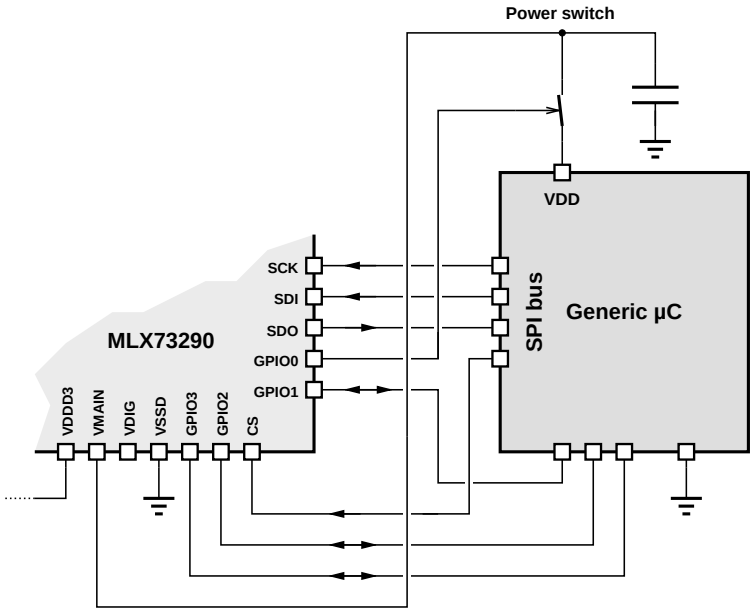
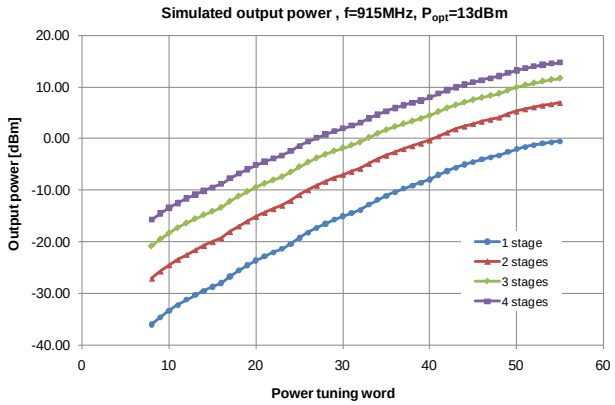


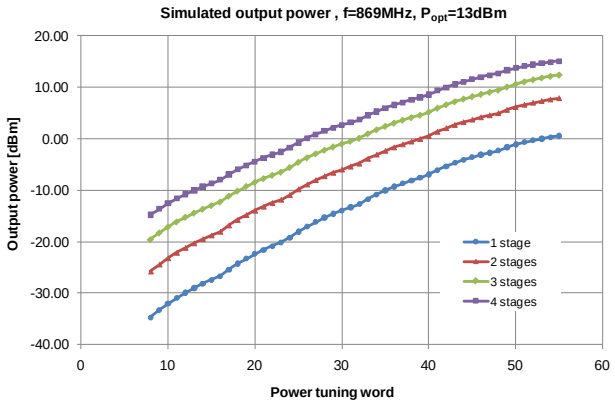
Figure 15: Micro-controller supplied through an external power switch

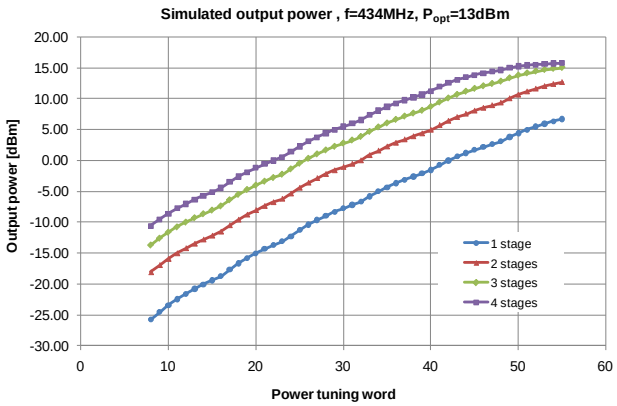
In that specific case, one of the GPIO signals can be used to control an external power switch which is useful to cut down the residual power consumption of the microcontroller. Note that the chip select wire of the SPI interface has been defined *active high* specifically for this application. Indeed, this avoids having the MLX73290-A "selected" when the microcontroller power is down.

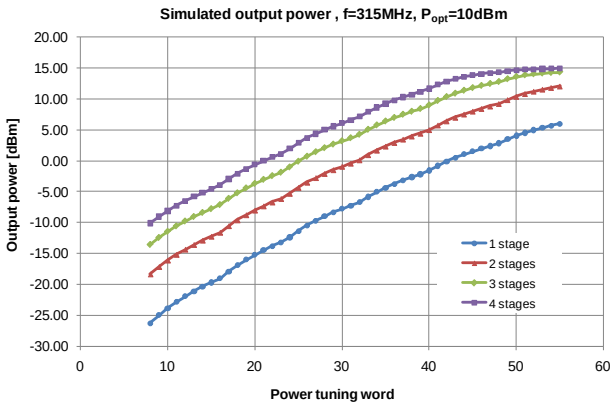
8 Performance Plots

8.1 Simulated output power









8.2 Spectrum Plots

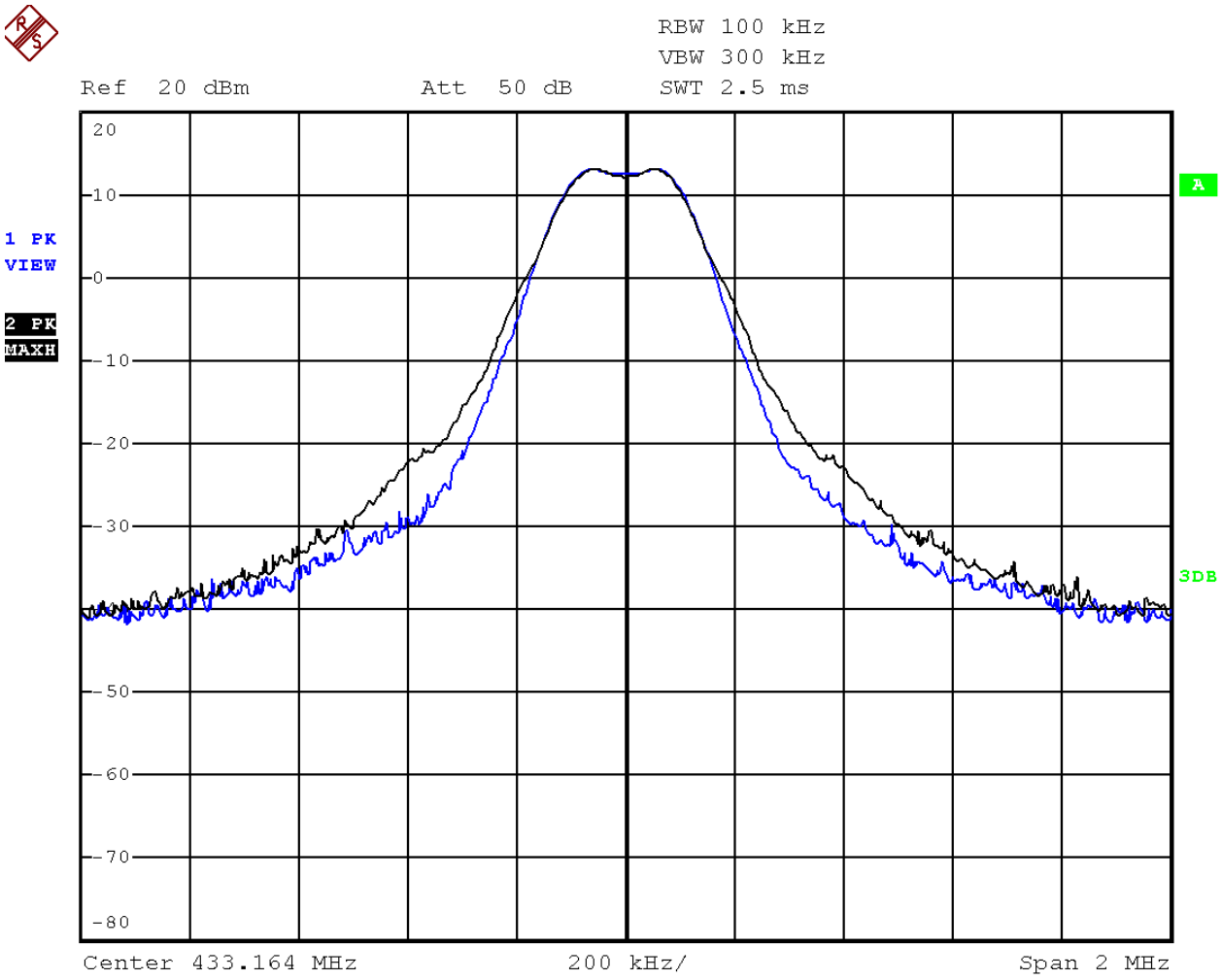


Figure 19: FSK (black) and GFSK (blue) spectrum at 250kbps, ±50kHz deviation

8.3 Eye Diagram

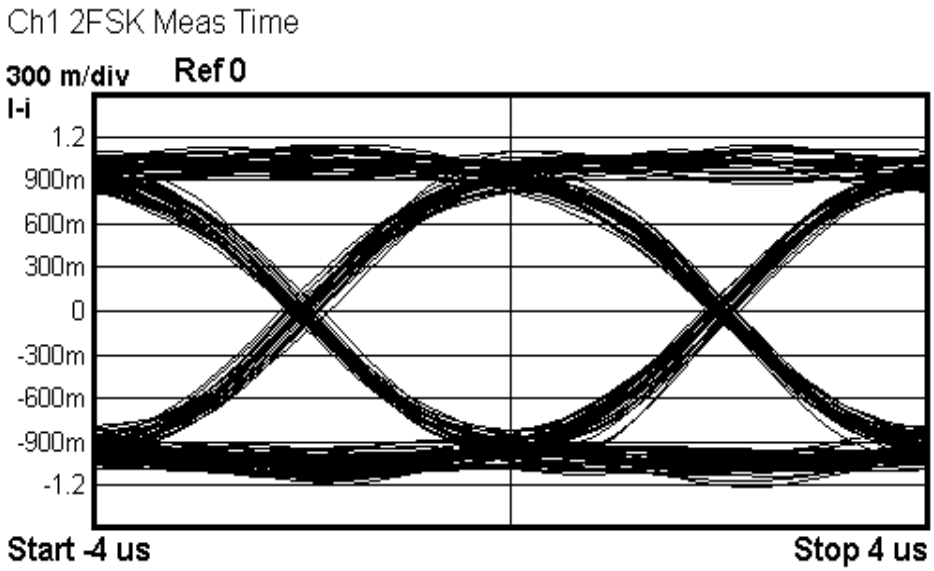


Figure 20: 250kbps GMSK transmit signal eye diagram at 868MHz

8.4 Phase Noise

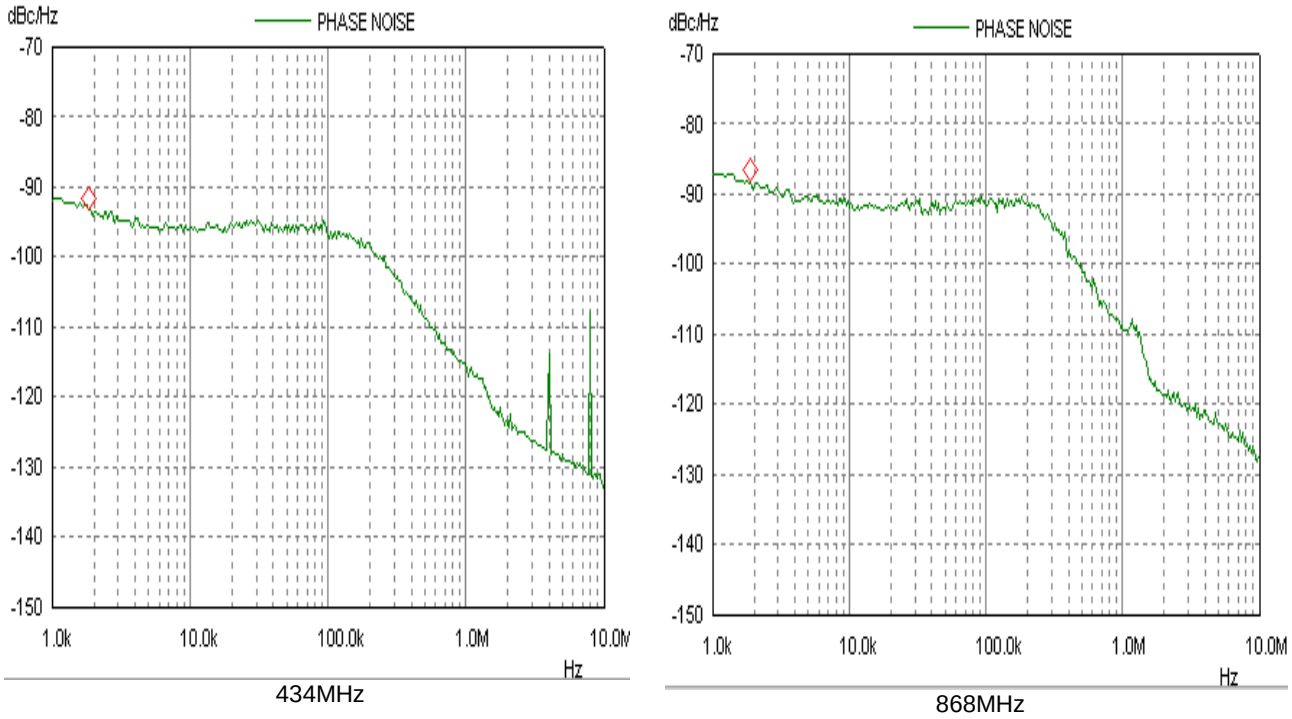


Figure 21: 434MHz and 868MHz phase noise plots

9 Manufacturability of Melexis Products with Different Soldering Processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

10 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

11 Package Information

The device MLX73290-A is RoHS compliant.

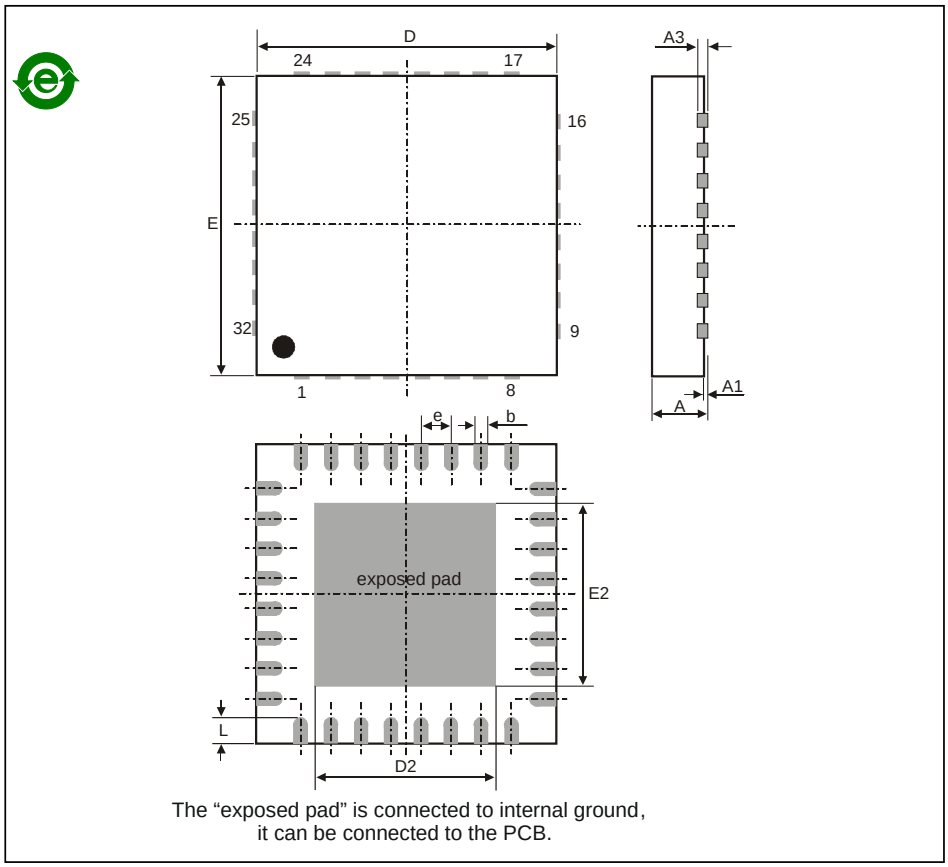


Figure 16: 32L QFN 5x5 Quad

all Dimension in mm										
	D	**E**	**D2**	**E2**	**A**	**A1**	**A3**	**L**	**e**	**b**
min	4.75	4.75	3.00	3.00	0.80	0	0.20	0.3	0.50	0.18
max	5.25	5.25	3.25	3.25	1.00	0.05		0.5		0.30
all Dimension in inch										
min	0.187	0.187	0.118	0.118	0.0315	0	0.0079	0.0118	0.0197	0.0071
max	0.207	0.207	0.128	0.128	0.0393	0.002		0.0197		0.0118

Table 112: 32L QFN 5x5 Dimension

12 Disclaimer

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