Application Processor Lite *ApP Lite*™

TZ1041MBG

Technical Data sheet

Hardware Specification

Revision 1.0

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TOSHIBA CORPORATION

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Abbreviations

These specifications introduce a part of the abbreviation which they used.

BT Bluetooth™

BLE Bluetooth™ Low Energy

Notes

This document will be modified without further notice. Ensure that you refer to the latest version of the document when using the product. For information on the latest version, contact TOSHIBA technical support.

Conventions in this document

- The numerical values are expressed as follows.
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary number: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1, and S0 together.
- The characters surrounded by *[ ]* defines the register.
  Example: *[ABCD]*
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: *[XYZ1]*, *[XYZ2]*, and *[XYZ3]* to *[XYZn]*
- The bit range of a register is written like as [m:n].
  Example: Bit[3:0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: *[ABCD]*.EFG = 0x01 (hexadecimal), *[XYZn]*.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, don't use the read value.
- Properties of each bit in a register are expressed as follows.
  R: Read only
  W: Write only
  W1C: Write 1 Clear - The corresponding bit is cleared (= 0) when "1" is written to this bit.
  W1S: Write 1 Set - The corresponding bit is set (= 1) when "1" is written to this bit.
  R/W: Read and Write are possible.
  R/W0C: Read/Write 0 Clear
  R/W1C: Read/Write 1 Clear
  R/W1S: Read/Write 1 Set
  RS/WC: Read Set/Write Clear - Set after read operation, cleared after write operation.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "—," follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—," follow the definition of each register.

1. Summary

The TZ1041MBG is a product which belongs to the TZ1000 Series, a family of processors for wearable devices. The TZ1041MBG incorporates a high performance 32-bit ARM® Cortex®-M4F RISC processor with 288 KB SRAM and 1 MB NOR flash memory, a high resolution 24-bit ΔΣADC and a Bluetooth Low Energy controller all in one package. The package size is 6.7 mm × 8 mm and its compact size package contributes to designing of smaller wearable devices than the conventional ones.

The TZ1041MBG supports a variety of peripheral interfaces such as the USB Device mode, UART, SPI, and I^2C. These interfaces allow the TZ1041MBG to easily connected to the MEMS sensors with digital interfaces, such as atmospheric pressure sensors and moisture sensors. The TZ1041MBG also incorporates a 12-bit ADC and a 24-bit ΔΣADC. Without any special analog front-end devices, this 24-bit ΔΣADC allows the TZ1041MBG to be directly connected to a photo diode for pulse sensing, a photoelectric sensor and a wide variety of sensors, such as a gas sensor. This contributes to reducing the total system cost.

1.1. Features

- CPU Core
  - ARM Cortex-M4F running at up to 48 MHz
  - Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
  - ARM® Thumb®-2 instruction set
- Memories
  - 288 KB embedded SRAM
  - 1 MB NOR Flash integrated in same package
- System Functions
  - Embedded voltage linear and switching regulator for single supply operation
  - Brown-out Detectors
  - Crystal oscillators: 12 MHz main and USB, 26 MHz for Bluetooth controller and 32.768 kHz for RTC
  - High precision 4 MHz factory trimmed internal RC oscillator
  - Low power 32.768 kHz internal RC oscillator
- Peripherals
  - USB 2.0 Device: 12 Mbps, 1 port 4 bidirectional endpoints
  - Two Master/Slave I^2C interface up to 400 kbps
  - Two UART
  - Two SPI Master with Chip Selects Signals
  - One 4-channel ADC with 12-bit resolution
  - One 3-channel Delta-Sigma ADC with 24-bit resolution
  - Advanced Encryption System (AES) Engine with 128/192/256-bit key length
  - True random number generator
  - 24 general purpose IOs (GPIO)
  - Real-time Clock which supports calender mode
  - Watchdog timer
  - Four 16-bit Advanced Timer/Counter Channels with capture, compare and PWM mode
  - Two 32-bit Timer/Counter Channels
  - One 8 channels DMA controller
  - Bluetooth 4.1 Controller with RF
- Single Power Supply
  - Voltage range: 2.1 to 3.6 V.
- Packages
  - 136-ball P-LFBGA 6.7 × 8.0 mm, pitch 0.5 mm

2. Description

The TZ1041MBG is a product which belongs to the TZ1000 Series, a family of processors for wearable devices. The TZ1041MBG incorporates a high performance 32-bit ARM Cortex-M4F RISC processor with 288 KB SRAM and 1 MB NOR flash memory, a high resolution 24-bit ΔΣADC and a Bluetooth Low Energy controller all in one package. The Cortex-M4F processor consists of a floating point processor unit, a memory protection unit, and a flexible interrupt controller. It supports many kinds of real time OS.

The TZ1041MBG can select the most suitable power supply voltage and circuit to its operating frequency. Users can achieve the lowest power consumption in their applications to use the power saving mode.

The TZ1041MBG includes a low power and as large capacity as 288 KB of SRAM, and a 1 MB NOR flash memory which is used to store program codes and data. The TZ1041MBG can realize an activity meter and other devices without any other components.

The Bluetooth Low Energy controller supports up to GATT profile. So, the Bluetooth protocol operations consume no additional processor resources of the SRAM, the storage means, and the process executions. The power supply to the Bluetooth controller can be shut down separately. No power can be consumed when it does not operate.

An AES engine and a random number generator are incorporated for a security function. The AES complies with FIPS (Federal Information Processing Standard) Publication 197, Advanced Encryption Standard. It can select a key length among 128 bits, 192 bits, and 256 bits, and executes the encryption and decryption without any processes of the processor.

The random number generator has passed the random number test of NIST SP800-22 (National Institute of Standards and Technology Special Publication 800-22), and it can be used for the bases of keys and others.

The 8 channel DMA controllers perform the data transfer between the SRAM and the peripheral such as the UART or between the SRAMs without any processes of the processor. The data transfer engine (SRAMC) in the SRAM controller enables the data transfer between the SRAMs without passing the data buses.

The TZ1041MBG also incorporates a 12-bit ADC and a 24-bit ΔΣADC. Without any special analog front-end devices, this 24-bit ΔΣADC allows the TZ1041MBG to be directly connected to a photo diode for pulse sensing, photoelectric sensors with small output voltage like for ECG measure application and a wide variety of sensors, such as a gas sensor. This contributes to reducing the total system cost.

3. Features

3.1. Block Diagram

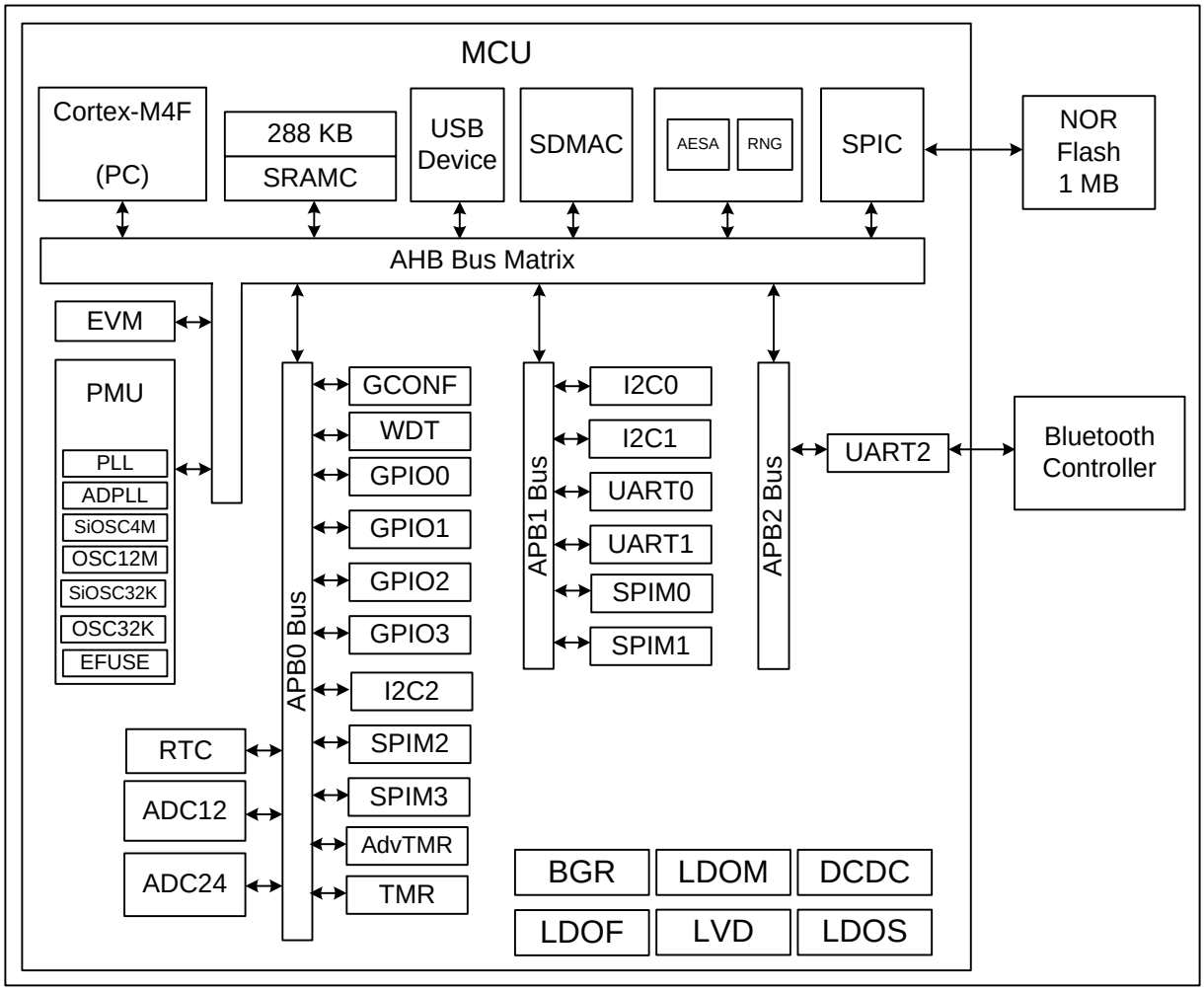


Figure 3.1 Block Diagram

3.2. MCU Summary

3.2.1. Configuration Summary

Table 3.1 Configuration Summary

Feature	TZ1001MBG	TZ1041MBG	TZ1011MBG	TZ1031MBG	TZ1021MBG
Number of Pins	136		153	153	110
Max Frequency	48 MHz				
SRAM	288 KB				
NOR Flash	1024 KB (*1)				
GPIO	24(32) (*2)				32
Wakeup Interrupts	8(13) (*2)				13
I^2C	2(3) (*2)		3		
UART	2(3) (*2)				3
DMA Channels	8				
AES Engine	1				
True Random Number Generator	1				
SPI	3(4) (*2)				4
Quad SPI for Flash connection	0(1) (*2)				
16-bit Timer(PWM)	4				
32-bit Timer	2				
Watchdog Timer	1				
Power Manager	1				
Oscillators	32.768 kHz Silicon Oscillator 32.768 kHz Oscillator 4 MHz Silicon Oscillator 12 MHz Oscillator				
12-bit ADC	4				
24-bit ADC	3				
USB Device	1				
Accelerometer	1	0	1		0
Gyroscope	0		1		0
Magnetometer	0		1	0	
Bluetooth Low Energy Controller	1				0
Packages	P-LFBGA				P-VFBGA

*1: NOR Flash is connected internally via SPI.

*2: Number inside the bracket means the channel counts of internal MCU.

3.2.2. CPU Core

ARM Cortex-M4F processor
Instruction set Architecture: ARMv7E-M architecture
Single Precision floating point unit with IEEE 754 compliant
Supports SIMD and MAC DSP extension instructions
Thumb2 instruction set
Memory protection unit
Integrated bit manipulation instructions & bit banding
Operating Frequency: selectable from 32.768 kHz to 48 MHz
Debug function: ARM® CoreSight™ component
V7 debug architecture with JTAG debug port

3.2.3. Memories/Storage

SRAM
Memory size: 288 KB

NOR Flash
Memory size: 1 MB
Interface: SPI with application execute-in-place/DMA engine

3.2.4. System

Embedded voltage linear and switching regulator (1.2 V/1.1 V/1.0 V/0.9 V)
Embedded LDO (1.7 V)
High precision 4 MHz internal Silicon oscillator
Low power 32.768 kHz internal Silicon oscillator
Analog PLL up to 48 MHz for whole system and USB with reference clock 12 MHz
Digital PLL up to 48 MHz with reference clock 32.768 kHz

AES Accelerator (AESA)
AES accelerator engine with 128, 192, 256-bit key length
Compliant with FIPS 197 (Advanced Encryption Standard)
Encryption/Decryption with dedicated DMA engine
Supported 3 block cipher modes of operation (ECB, CBC, CTR)

True Random Number Generator (RNG)
Generates 32-bit true random number
NIST SP800-22 (NIST special publication 800-22) passed

Real Time Clock (RTC)
- Clock (hour, minute and second)
- Calendar (month, week, date and leap year)
- Selectable 12 (am/pm) and 24 hour display
- Time adjustment + or – 30 seconds
- Alarm interrupt
- Periodic interrupt
- BCD format for calendar data

Watch Dog Timer (WDT)
- 32-bit Timer with interrupt and reset when timeout

DMA Controller (SDMAC)
- 8 Channels
  - Each channel has source and destination pair
- Programmable source and destination addresses
  - Addressing mode can be increment, decrement or no change
  - Handshaking interfaces for source and destination peripherals
    - UART, I^2C, SPI, ADC12, ADC24

Timer (TMR)
- 32-bit down Counter
  - Selectable 32-bit/16-bit count mode
- Two Channels
- Operation Mode
  - One shot timer mode
  - Periodic timer mode
  - Free running timer mode
- Pre-scale unit generating timer clock
  - (×1, ×1/16, ×1/256)

Advanced Timer (AdvTMR)
- 16-bit down Counter
  - Selectable 16-bit/8-bit count mode
  - Input capture function for each channel
  - Output compare function for each channel
- Four Channels
- Operation Mode
  - One shot timer mode
  - Periodic timer mode
  - Free running timer mode
- Pre-scale unit generating timer clock
  - (×1, ×1/2, ×1/4, ×1/8, ×1/32, ×1/128, ×1/512, ×1/1024)
- Timing selection of input capture
  - (Pulse, Rising edge, Falling edge, both edges)
- PWM (Pulse Width Modulation) operation that uses output compares function

3.2.5. Peripherals

SPI for general purpose (SPIM)
- Four Channels
  - One channel (Ch2) reserved
  - Three Channels (Ch0, Ch1 and Ch3) free for external connections
- Master Function
- SPI Clock up to 6 MHz
- FIFO Depth
  - Ch0, Ch1: RX FIFO 8, TX FIFO 8
  - Ch2, Ch3: RX FIFO 8, TX FIFO 2

SPI for NOR flash connection (SPIC)
- Quad SPI Clock up to 48 MHz
- Application eXecute-In-Place (XIP)
- Hardware image transferring feature to internal SRAM
- Programmable source and destination address

UART (UART)
- Three Channels (one channel (Ch2) reserved for BLE controller connections)
  - Two channels (Ch0 and Ch1) free for external connection
  - One channel with CTS/RTS
- FIFO Depth
  - RX FIFO 12, TX FIFO 8
- Programmable baud rate generator
  - Input reference clock; up to 16 MHz
  - Data rate up to 1 Mbps
  - Division of reference clock by (1×16) to (65535 ×16)
- Hardware flow control
- Fully-programmable serial interface characteristics
  - Data can be 5, 6, 7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation

I^2C
- Three Channels (one channel (Ch2) reserved)
- Transfer mode; Standard mode (100 kbps), Fast mode (400 kbps)
- Master or slave I^2C operation
- 7-bit or 10-bit addressing
- 7-bit combined format transfers
- Bulk transfer mode
- FIFO Depth
  - RX FIFO 6, TX FIFO 6

USB

- Compliant with Universal Serial Bus Specification revision 2.0
- Supports Full Speed (12 Mbps)
- One port, four endpoints
  - Endpoint 1-3 can be configured as interrupt/bulk transfer mode
- Internal DMA Controller

GPIO

- 32 Pins
  - 8 pins for internal connections (i.e. sensor interrupt)
  - 24 pins free for external connections
- Individually programmable as input or output
- Interrupt generation capability from a transition or level condition
- Pull-up/pull-down resistors configurable

12-bit Analog to Digital Convertor (ADC12)

- Successive approximation type
- 12 bits resolution
- Conversion time: 17 cycles at 1 to 12 MHz
- Four channel analog inputs
- Selectable conversion mode (Single/One-time scan/Cyclic scan)
- FIFO Depth 8 for each channel

24-bit Analog to Digital Convertor (ADC24)

- Delta-Sigma type up to 24-bit resolution
- Three channel differential analog inputs
- Conversion time: 4130 cycles at 24-bit resolution
- Selectable conversion mode (Single/One-time scan/Cyclic scan)
- FIFO Depth 16 for each channel
- Configurable analog front end

3.3. Bluetooth Low Energy summary

The TZ1041MBG complies with 2.4 GHz wireless communication Bluetooth V4.1 Low Energy standards. The TZ1041MBG includes the RF and Baseband parts, and supports the HCI (Host Control Interface) function and the Profile function for the Low Energy. The TZ1041MBG performs easily the low power Bluetooth applications.

3.3.1. Feature

- Compliant with Bluetooth Ver4.1 Low Energy standards
  - Bluetooth Baseband circuit
  - Bluetooth RF circuit
  - ARM® ARM7TDMI-S™ Core
  - Mask ROM for Bluetooth programs
  - Work RAM for processing Bluetooth Baseband
- General purpose I/O (9 ports) for test
- Basic operation clock input (26 MHz)
  - Oscillation circuit for an external oscillator
- Sleep clock input (32.768 kHz)
  - External clock input
  - Oscillation circuit for an external oscillator
- Supporting a sleep mode and a deep sleep mode

3.3.2. System Diagram

The diagram of the internal blocks and the connections to peripherals is shown as follows.
The basic operation clock frequency is 26 MHz, and the sleep clock frequency is 32.768 kHz.
The UART is the interface to the CPU.

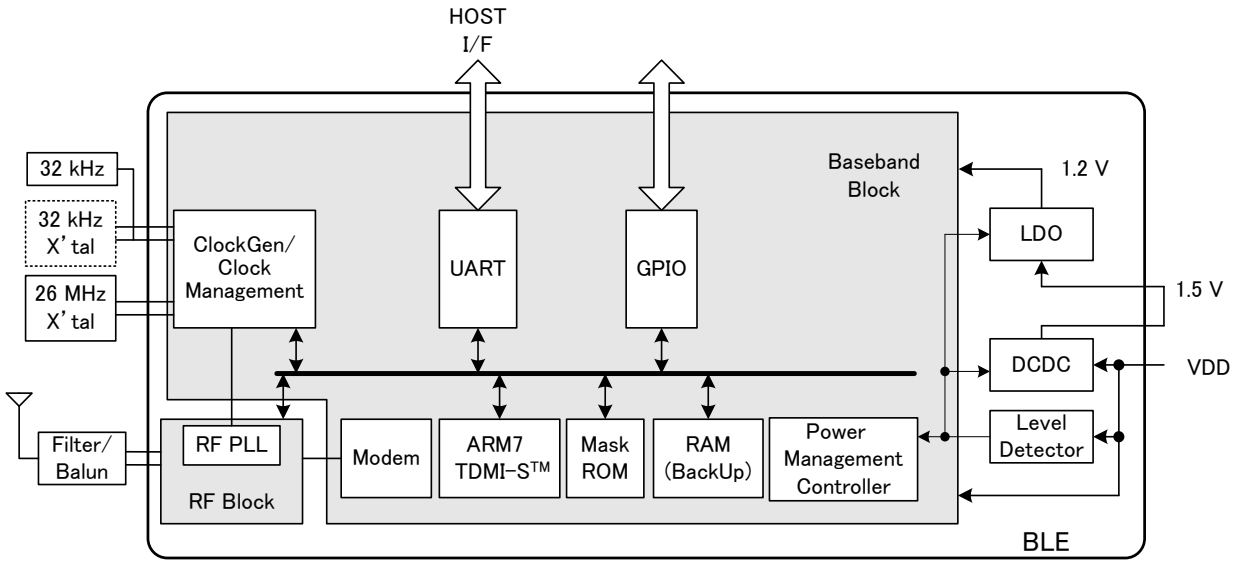


Figure 3.2 Internal blocks and connections to peripherals

3.4. Internal Flash Memory summary

The TZ1041MBG includes an NOR-Flash memory chip in the package. The Flash memory is connected to the SPI controller (SPIC) in the package. The power supply of the Flash memory is provided on the TZ1041MBG pin and it is through the LDO (Low Drop Out regulator) chip in the package. The power supply or shut down is controlled by software.

The direct access mode is supported to program the Flash memory. When the memory is started up in this mode, the signals between the Flash memory and the SPIC are connected to the external pins of the TZ1041MBG.

The feature of the Nor-Flash memory included in the TZ1041MBG is as follows.

- Flash memory type: SPI-Flash memory
- Memory capacity: 8 Mbits (1 MB)
- Supply voltage: 1.65 to 1.85 V
- Access modes: Single, Dual and Quad modes

4. Operation

4.1. Power Supply Overview

The overview of the TZ1041MBG power supply composition is shown in Figure 4.1.

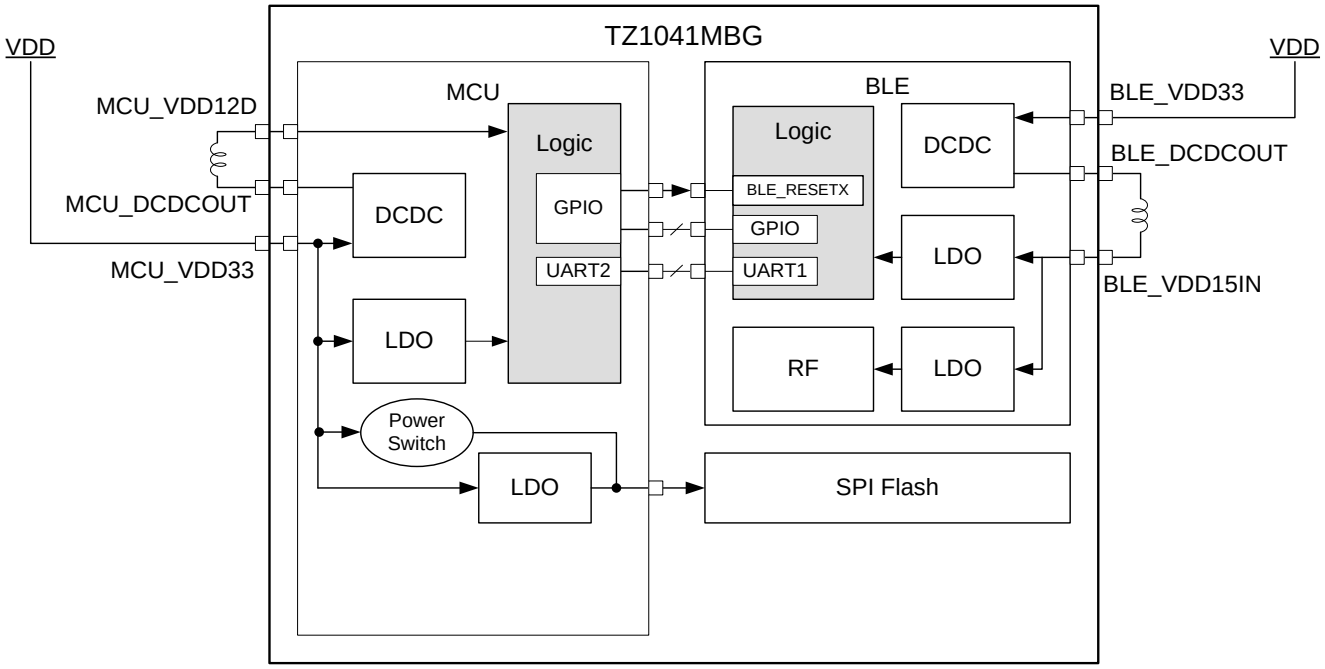


Figure 4.1 TZ1041MBG Power Supply Overview (with DCDC)

The MCU chip and the BLE chip have DCDC/LDO respectively, and operate independently.

The MCU chip performs the MCU chip's own power supply control, and supply the power to the SPI Flash and each sensors.

Refer to chapter 4.5 for detail of MCU power management function.

The BLE chip has the original Power Management function which become independent of the MCU chip. When the MCU chip controls the Power Management of the BLE chip, the HCI Command via the UART I/F and the interrupt signal via GPIO are used. Moreover, system reset terminal BLE_RESETX of the BLE chip is controlled by the GPIO of the MCU chip. Refer to the "chapter 3.3. Bluetooth Low Energy summary" and the reference manual Bluetooth Low Energy for the details and the control method of the Power Management function of the BLE chip.

4.2. Clock/Reset Overview

The overview of the TZ1041MBG clock/reset composition is shown in Figure 4.2.

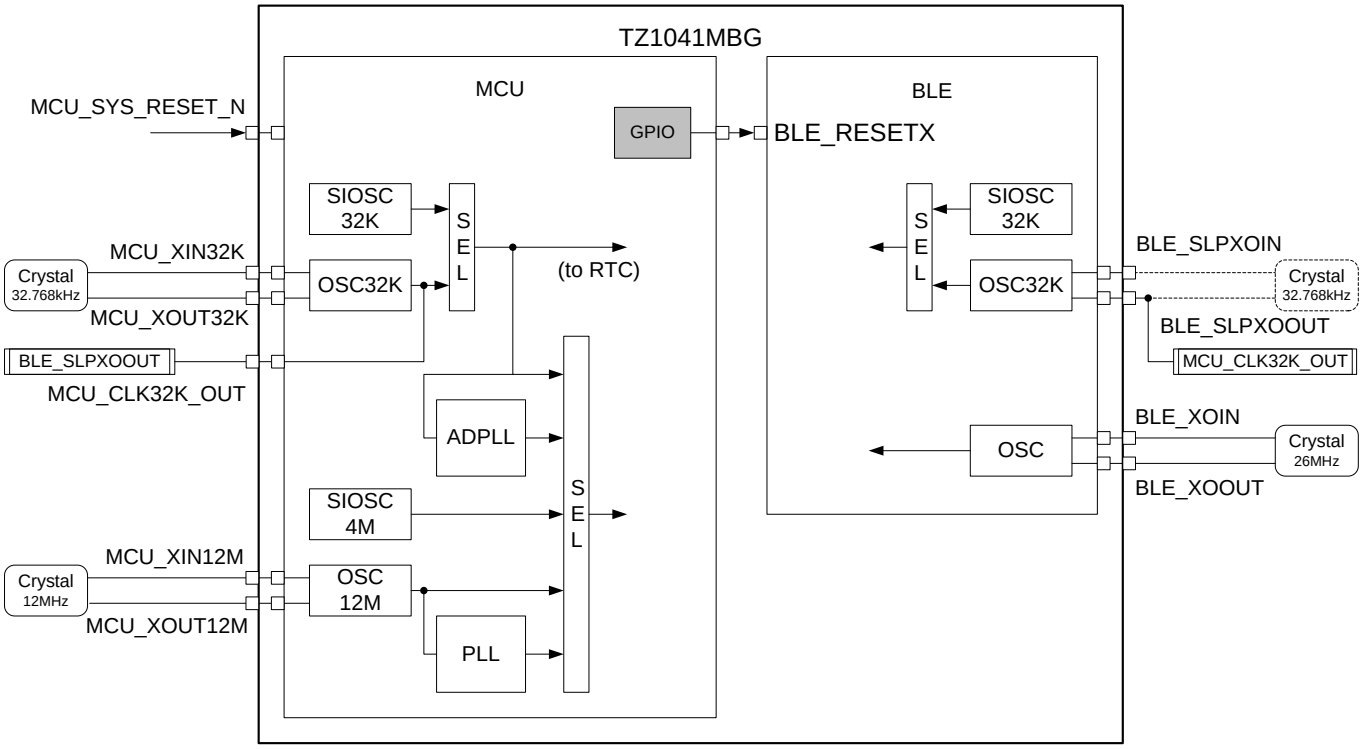


Figure 4.2 TZ1041MBG Clock/Reset Overview

4.2.1. MCU Clock Source

One of the flowing 6 clocks can be clock source of MCU internal clock system.

- OSC32K
  - Clock from external crystal oscillator.
  - Frequency: 32.768 kHz
- SIOSC32K
  - Clock from embedded silicon oscillator.
  - Frequency: 32.768 kHz
  - Trimming is mandatory for accurate frequency.
  - This clock can be used as RTC clock same as OSC32K
- SIOSC4M
  - Clock from embedded silicon oscillator.
  - Frequency: 4 MHz
  - Trimming is mandatory for accurate frequency.
- ADPLL
  - All digital PLL output using OSC32K or SIOSC32K as reference clock.
  - Reference clock needs to be activated when ADPLL is selected.
  - Frequency: 48 MHz
- OSC12M
  - Clock from external crystal oscillator.
  - Frequency: 12 MHz
- PLL
  - PLL output using OSC12M as reference clock.
  - Reference clock needs to be activated when PLL is selected.

– Frequency: 12/24/36/48 MHz can be switched.

Refer to "Reference Manual MCU power management unit" for details.

4.2.2. BLE Clock Source

The clock of the BLE chip is classified into two, a sleep clock (32.768 kHz) system and the clock (26 MHz) for basic motion.

The source of the sleep clock can be selected from OSC32K and SIOSC32K.

- OSC32K
  - Clock from external crystal oscillator or external clock source.
  - Frequency: 32.768 kHz
- SIOSC32K
  - Clock from embedded silicon oscillator.
  - Frequency: 32.768 kHz
  - Trimming is mandatory for accurate frequency.
  - This clock can be used as RTC clock same as OSC32K

The source of the clock for basic motion is OSC.

- OSC
  - Clock from external crystal oscillator.
  - Frequency: 26 MHz

4.3. MCU Power-up Sequence

Power-up sequence starts by deasserting a MCU_SYS_RESET_N terminal after supply of MCU_VDD33. A MCU_SYS_RESET_N terminal should be deasserted when the voltage of MCU_VDD33 is more than 1.8 V.

MCU_SYS_RESET_N from external input port reset entire system. After deassert of it, power up and startup sequence run to boot.

- SPI Flash Internal LDO mode (BOOTMODE3 = 0)

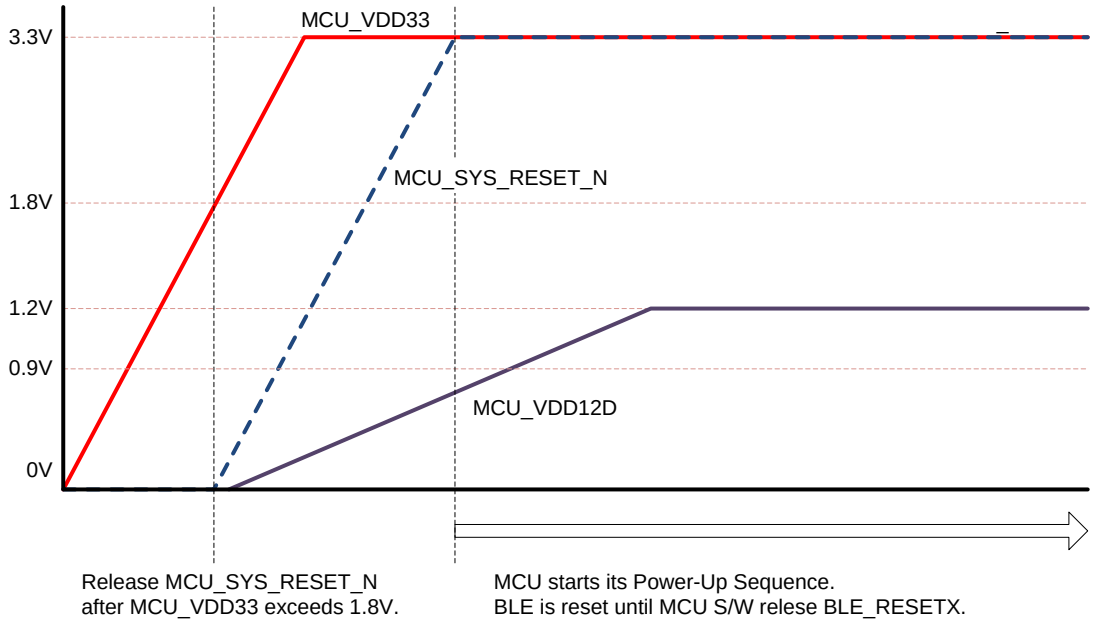


Figure 4.3 MCU Power-up Sequence

4.4. BLE Power-up Sequence

The GPIO and the UART I/F are connected between the MCU chip and the BLE chip, and control the system reset of the BLE chip from MCU chip. When the power supply is started to the MCU chip, the reset release of the BLE chip is performed by S/W on the MCU chip after the MCU chip power-up sequence. The BLE chip starts supply of an internal core power supply, and boots up. Completion of the BLE power-up sequence will transmit Command Complete (NOP) via the UART I/F from the BLE chip.

Table 4.1 BLE Power-up Sequence

MCU chip IO	Dir.	BLE chip IO	Description
MCU_GPIO_28	⇨	RESETX	System reset
MCU_GPIO_31	⇨	GPIO0 / RequestWakeUp	IO setting change by HCI Command is required.
MCU_GPIO_30 (w/WakeUp)	|	GPIO1 / HostWakeUp	IO setting change by HCI Command is required.
MCU_GPIO_29	|	GPIO2 / Status	IO setting change by HCI Command is required.
MCU_UA2_RXD	|	GPIO3 / UART1-TX	—
MCU_UA2_TXD	⇨	GPIO4 / UART1-RX	—
MCU_UA2_CTS_N	|	GPIO5 / UART1-RTSX	IO setting change by HCI Command is required.
MCU_UA2_RTS_N	⇨	GPIO6 / UART1-CTSX	IO setting change by HCI Command is required.

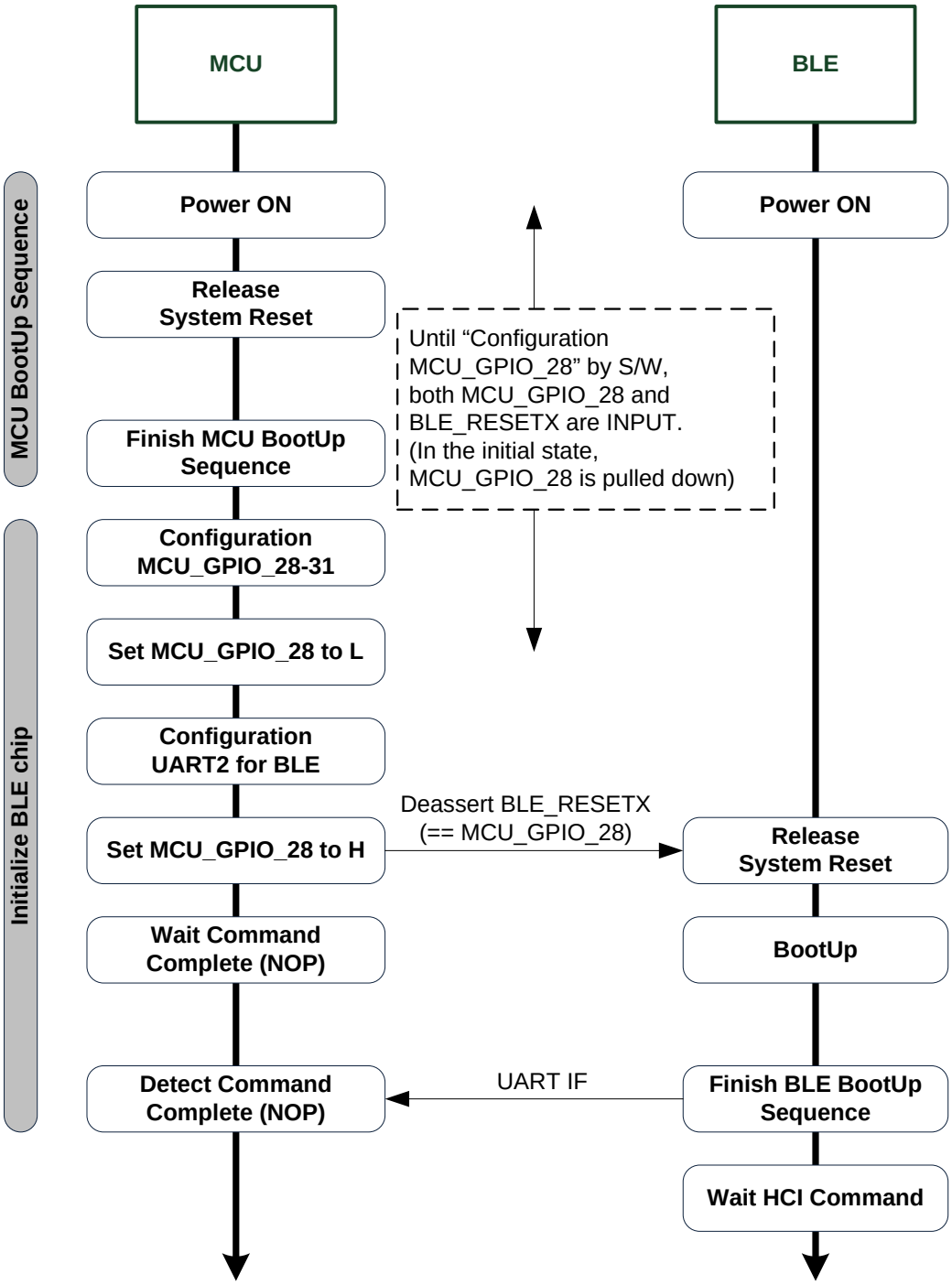


Figure 4.4 BLE Power-up Sequence

4.5. MCU Power Management Summary

MCU chip supports multiple power configurations to allow the user to optimize its power consumption in deferent use cases. Power Management Unit (PMUHV/PMULV) implements different solutions to reduce the power consumption.

- The Power Mode intended to reduce the logic activity (whole or a part of clock stop).
- The Voltage Scaling Mode intended to scale the power configuration (voltage scaling of the regulator).

Following diagram are images of two solutions (Power Mode and Voltage Mode)

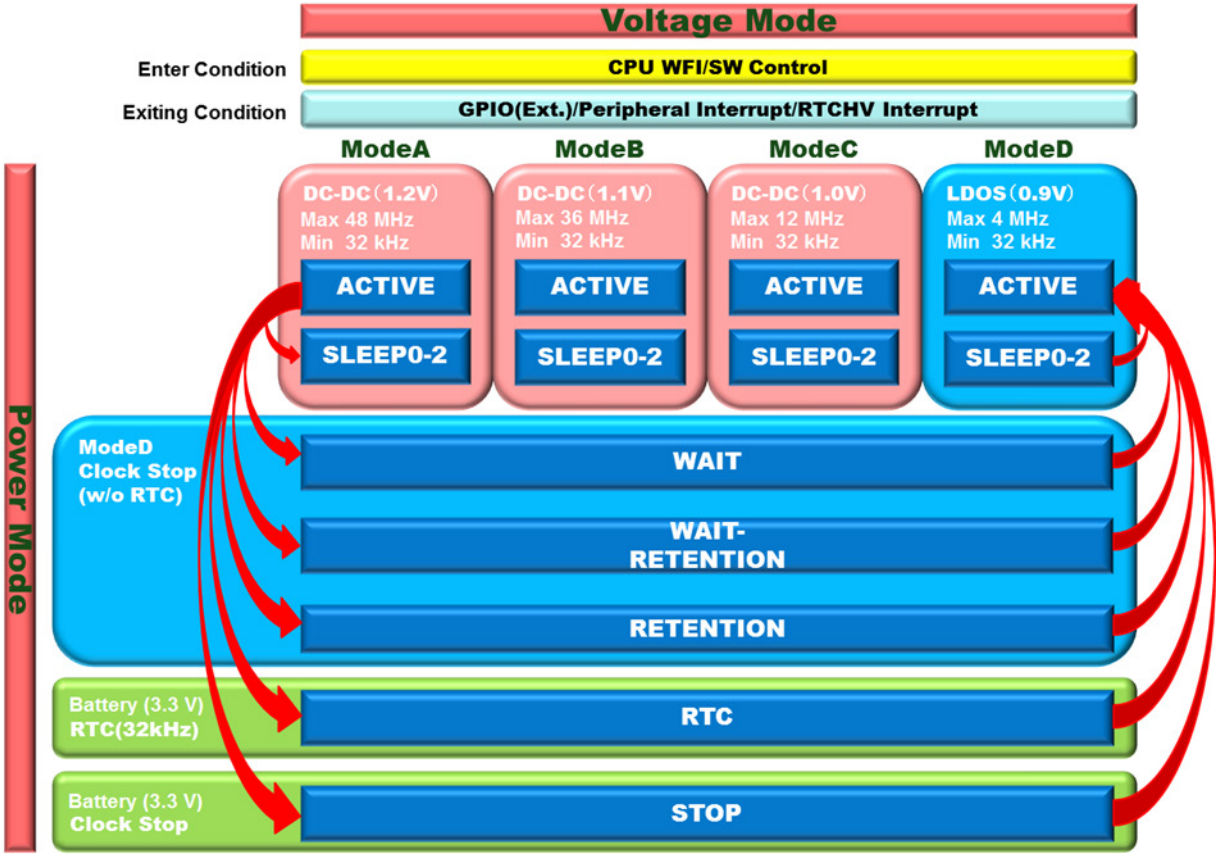


Figure 4.5 MCU Power Mode and Voltage Scaling Overview

Table 4.2 MCU Power Mode and Voltage Mode overview

Power Mode	Description	Voltage Mode	CPU Clock	AHB Clock	APB Clock	RTC Clock	Power Domain
ACTIVE	Active Mode	ModeA-D	Run	Run	Run	Run	All ON (*1)
SLEEP0	CPU is stopped by WFI Fastest wake up time	ModeA-D	Stop	Run (*1)	Run (*1)	Run	All ON (*1)
SLEEP1	CPU is stopped, and AHB Clock is stopped Fastest wake up time	ModeA-D	Stop	Stop	Run (*1)	Run	All ON (*1)
SLEEP2	CPU is stopped, and AHB/APB Clock is stopped Fastest wake up time	ModeA-D	Stop	Stop	Stop (*1)	Run	All ON (*1)
WAIT	All clock source are stopped. CPU and all peripherals are stopped except the rtc running with the 32.768 kHz clock if enabled.	ModeD	Stop	Stop	Stop	Run	PM_B:ON PS0_B: WAIT PS1_B: WAIT (*2) PS2_B: WAIT (*2) Other: ON
WAIT-RETENTION	Same as WAIT mode but many logic is retained except PU_B and PM_B domain	ModeD	Stop	Stop	Stop	Run	PM_B: ON PS0_B: WAIT PS1_B: WAIT (*2) PS2_B: WAIT (*2) PU: OFF Other: RET
RETENTION	Lowest power configuration where the logic is retained except PU_B domain	ModeD	Stop	Stop	Stop	Run	All RET (*3) PU_B: OFF
RTC	PM_B domain is power off, PA_B domain kept power with running 32.768 kHz clock.	—	Stop	Stop	Stop	Run	PA_B: ON Other: OFF
STOP	PM_B domain is power off, PA_B domain kept power and 32.768 kHz clock is stopped.	—	Stop	Stop	Stop	Stop	PA_B: ON Other: OFF

*1: It can be possible to shut off a part of power domain.

*2: It can be possible to shut off its power domain.

*3: It can be possible to shut off whole power domain except PM_B domain - RET means Retention.

Refer to the reference manual MCU Power Management Unit for detail of MCU power management function.

4.6. BLE Power Management Summary

The power mode of the MCU chip and the BLE chip can be set independently. The return to the active mode of one chip can be triggered by another using the GPIO signals.

The following settings should be done to the MCU chip to detect the return instruction to the active mode issued by the BLE chip before the MCU chip transits to the low power dissipation modes.

- SLEEP0/1
  The interrupt detection on the MCU_GPIO_30 pin should be enabled by the GPIO3 setting.
  SLEEP2, WAIT, WAIT-RETENTION, and RETENTION
  The interrupt detection of the GPIO3 does not operate in these modes.
  The interrupt or WakeUp on the MCU_GPIO_30 pin should be enabled by the PMU setting.
- RTC and STOP
  - In the case that the BLE chip operates at the mode transition.
    If the BLE chip operates at the transition to the RTC or STOP mode, the MCU_GPIO_28 pin should maintain High not to reset the BLE chip. This is done by the PMU *[CTRL_IO_AON_1]*.CTRL_IO_AON_PM_LATI setting. The interrupt or WakeUp on the MCU_GPIO_30 pin should be enabled by the PMU setting.
    At the return from these modes, the MCU_GPIO_28 pin should be set to become High by the GCONF and GPIO3 settings. Then, the IO maintaining function should be released by clearing the PMU *[CTRL_IO_AON_1]*.CTRL_IO_AON_PM_LATI. It is noted that if the clear is done before, the reset is asserted to the BLE chip.
  - In the case that the BLE chip does not operate at the mode transition.
    If the BLE chip does not operate at the transition to the RTC or STOP mode, the MCU_GPIO_28 pin should be set to Low and the reset is enabled to the BLE chip.

The power mode setting to the BLE chip can be done by the HCI command from the MCU chip. For detail, refer to the software specification of the BLE chip.

4.7. Power-Mode Combination

- The GPIO terminal between MCU chip and BLE chip has the following roles.
- RequestWakeUp (BLE_GPIO0 / MCU_GPIO_31)
  It is used when MCU chip controls Power Mode of the BLE chip (It is made to return to Active mode).
- HostWakeUp (BLE_GPIO1 / MCU_GPIO_30) It is used when controlling Power Mode of MCU chip (it is made to return to Active mode).
- Status (BLE_GPIO2 / MCU_GPIO_29)
  The Power Mode state of the BLE chip is notified to the MCU chip.

When communication is needed from MCU chip to BLE chip, Status (GPIO_29) is checked, and if required, the BLE chip will be returned to Active mode by RequestWakeUp.

When communication is needed from BLE chip to MCU chip, HostWakeUp from BLE chip is notified to MCU chip. Interruption via GPIO by GPIO_30 and the WakeUp function of the PMU should be effectively set up by S/W on the MCU chip.

Refer to the reference manual Bluetooth Low Energy for details of communication between the MCU chip and the BLE chip.

4.8. SPI Flash operation

4.8.1. Block Diagram

The connection diagram of the Flash memory in the TZ1041MBG is shown in Figure 4.6.

The signals of the Flash memory are connected to the SPIC. When the memory is started up in the direct access mode, the signals are connected to the external pins of the TZ1041MBG. The start-up setting is BOOTMODE[4:0] = 0b1*000 in the boot configuration.

The list of the signals of the Flash memory is shown in Table 4.3.

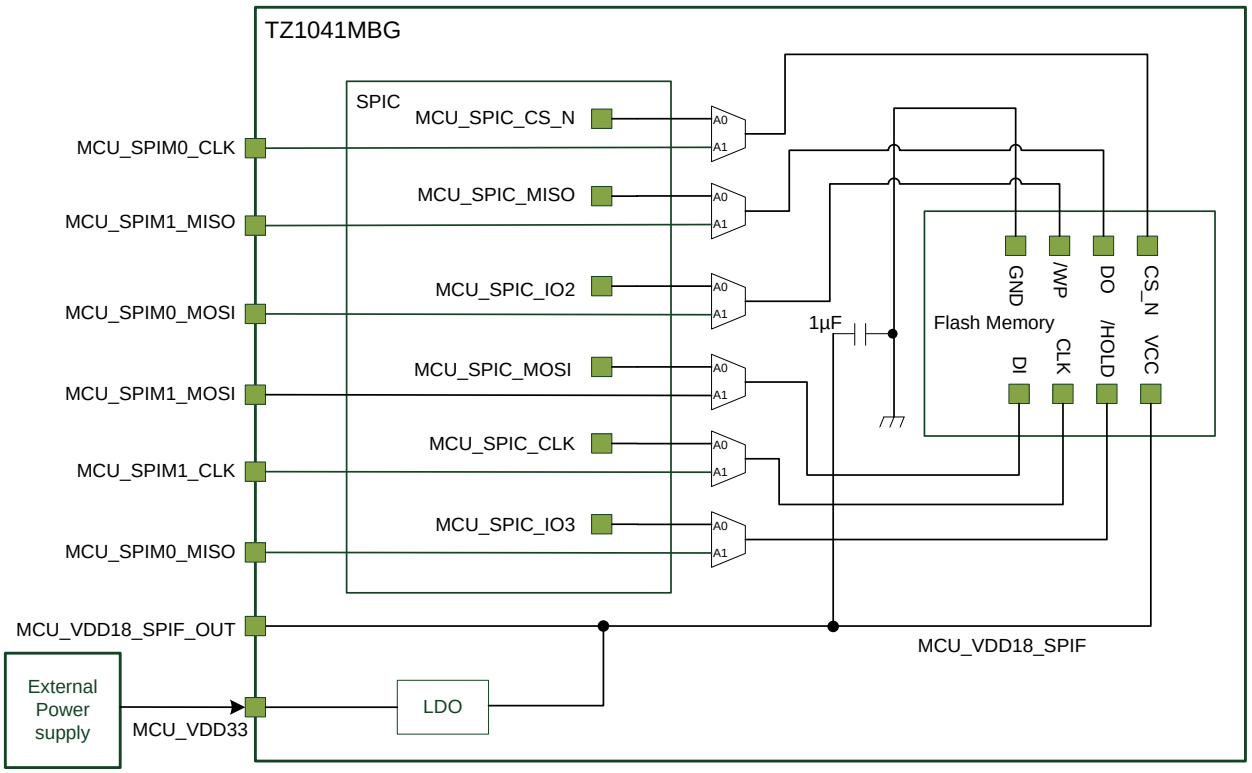


Figure 4.6 Internal block diagram

Table 4.3 Flash memory signals

Flash memory Pin	I/O	Connection in TZ1041MBG	Description
VCC	—	MCU_VDD18_SPIF_OUT	Power supply
CS_N	I	MCU_SPIC_CS_N	Chip select
/HOLD (IO3)	I/O	MCU_SPIC_IO3	Hold (IO3)
DO (IO1)	I/O	MCU_SPIC_MISO	Data output (IO1)
CLK	I	MCU_SPIC_CLK	Serial clock
/WP (IO2)	I/O	MCU_SPIC_IO2	Write protect (IO2)
DI (IO0)	I/O	MCU_SPIC_MOSI	Data input (IO0)
GND	—	GND	Ground

4.8.2. Flash Memory Control

4.8.2.1. Flash Memory Operation

The power mode of the Flash memory (power domain is PF) is linked with the power mode of the TZ1041MBG. For the detailed control, refer to the reference manual MCU Power Management Unit.

- ACTIVE/SLEEP/WAIT modes
  In these modes, the power is supplied to the Flash memory.
  Each domain power can be shut down separately by a register setting.
- RETENTION/RTC/STOP modes
  In these modes, the power is not supplied to the Flash memory.

4.8.2.2. Start-up Mode Setting for Flash Memory

The Flash memory supports the Single, Dual, and Quad access modes.

The access mode at the boot is the Single access mode as a default. If the following settings of 1 and 2 are done in advance, the Quad address mode can be started up at the boot.

(1) Flash memory QE bit setting
The QE bit setting is done to start up the Flash memory with the Quad mode.
The QE bit is written by the Flash programmer or by software after the boot with the Single access mode (QE bit default).
The built-in Flash memory in the TZ1041MBG has the QE bit is in both a volatile memory and non-volatile memory. The memory bit is selected by a command. Once the non-volatile memory is programmed, the start-up is done with the programmed setting.

Program the non-volatile memory: 0x06 to 0x01 (Status Register)
Write to the volatile memory: 0x50 to 0x01 (Volatile Status Register)

(2) Boot configuration setting (external pin setting)
BOOTMODE[2] 0b0: Internal Flash Single or Dual access mode
0b1: Internal Flash Quad access mode

4.8.3. Internal Flash Memory Programming

4.8.3.1. Flash Direct Access Mode (Internal Flash Programming Mode)

As a default, the signals of the Flash memory connected to the SPIC, not to the external pins. When a Flash programmer writes data to the internal Flash memory, the direct access mode (Flash memory programming mode) should be set.

If the boot configuration external pins BOOTMODE[4:0] = 0b1*000 are set and the TZ1041MBG is started up, the direct access mode is set and the Flash memory signals are connected to the external pins of the TZ1041MBG. For the detail of the boot configuration, refer to BootMode section in the reference manual MCU Overview.

In the direct access mode (internal flash programing mode), only Single access is supported (Dual and Quad access are NOT supported).

4.8.3.2. Flash Memory Programming Mode

- The power of the Flash memory is supplied inside of the package, not directly from the external. When the Flash memory is programmed, it is necessary that the power is supplied to the TZ1041MBG.
- 6 signals of the Flash memory are connected to the external pins in the direct access mode as shown in the following figure.
- On the TZ1041MBG system board, the 4 signals of the Flash memory should be connected through the SPIM0 and SPIM1 external pins to the 8-pin connector to which the Flash memory programmer is connected.

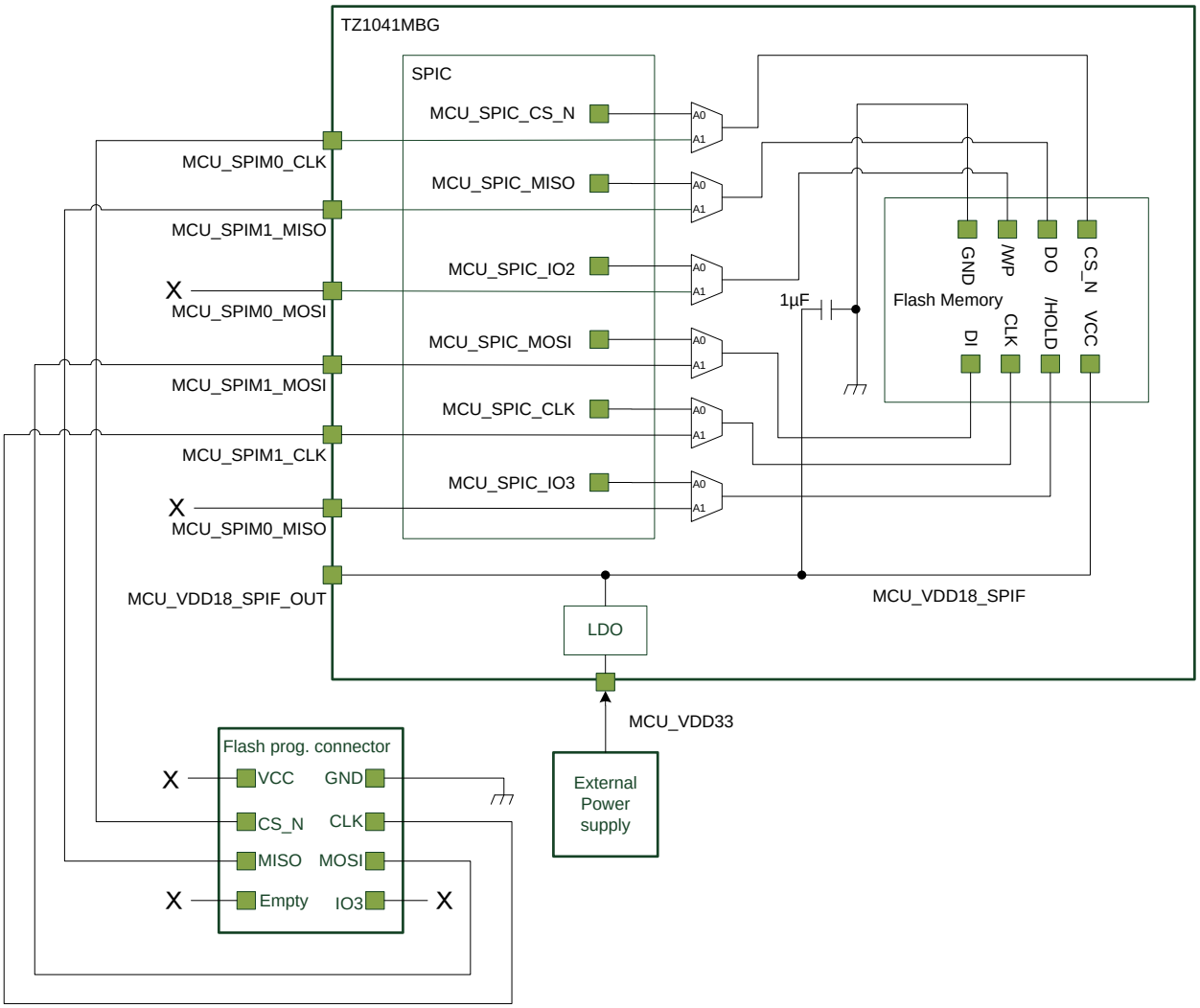


Figure 4.7 Flash memory programming connection

4.8.3.3. Flash Memory Programming Procedure

The following shows the Flash memory programming procedure using the Flash memory programmer on the TZ1041MBG system board.

(1) BOOTMODE[4:0] = 0b1*000 is set to start up the TZ1041MBG with the direct access mode (internal Flash memory programming mode).

(2) The Flash programmer is connected between the 8-pin connector on the system board and the PC which transfers the program.

(3) The power is supplied to the TZ1041MBG system board.
- The main power supply MCU_VDD33 in the TZ1041MBG provides the power to MCU_VDD_SPIF in the Flash memory.
- The Flash memory is supplied with the power and it is in the programming mode. (Refer to the figure in the next page.)
- The TZ1041MBG reset MCU_SYS_RESET_N is deasserted.
- The boot configuration setting is received and the TZ1041MBG starts up in the direct access mode (internal Flash memory programming mode).
- The signal destination of the Flash memory is switched to the external pins from the SPIC.
- The Flash programmer recognizes the Flash memory and the programming is enabled.

(4) The PC transfers a boot code and an application binary software (the Flash memory is programmed).
- The PC can set the Quad access mode (the register setting of the QE bit) through the Flash programmer, this time.

(5) After the Flash memory programming completes, the power of the system board is shut down and the Flash programmer is removed.

(6) BOOTMODE[4] = 0b0 is set for the TZ1041MBG to start up in the Normal mode - BOOTMODE[3:0] are specified by software. Then the power is supplied to the system board.

5. Package

5.1. Internal structure of TZ1041MBG package

The outline of the internal structure of the TZ1041MBG package is shown in "Figure 5.1 Internal Package diagram." The TZ1041MBG can basically be separated into MCU block, BLE block, Flash memory block.

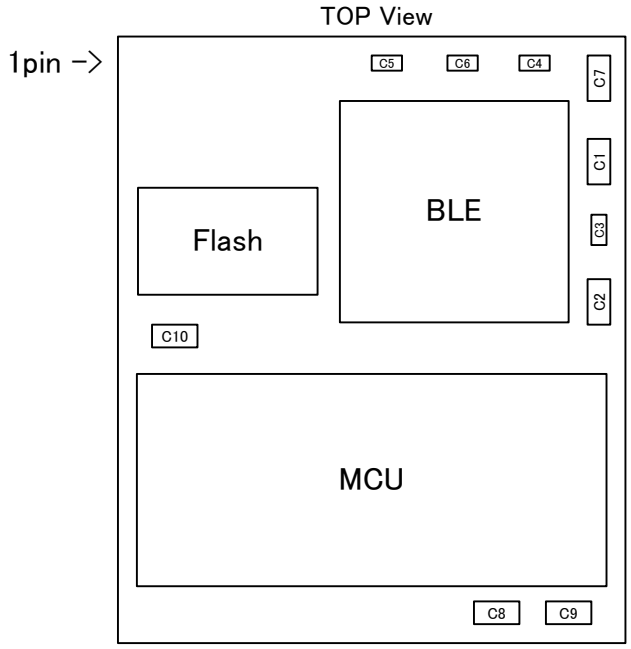


Figure 5.1 Internal Package diagram

Internal connection of each signal and power in the TZ1041MBG package is shown in Figure 5.2.

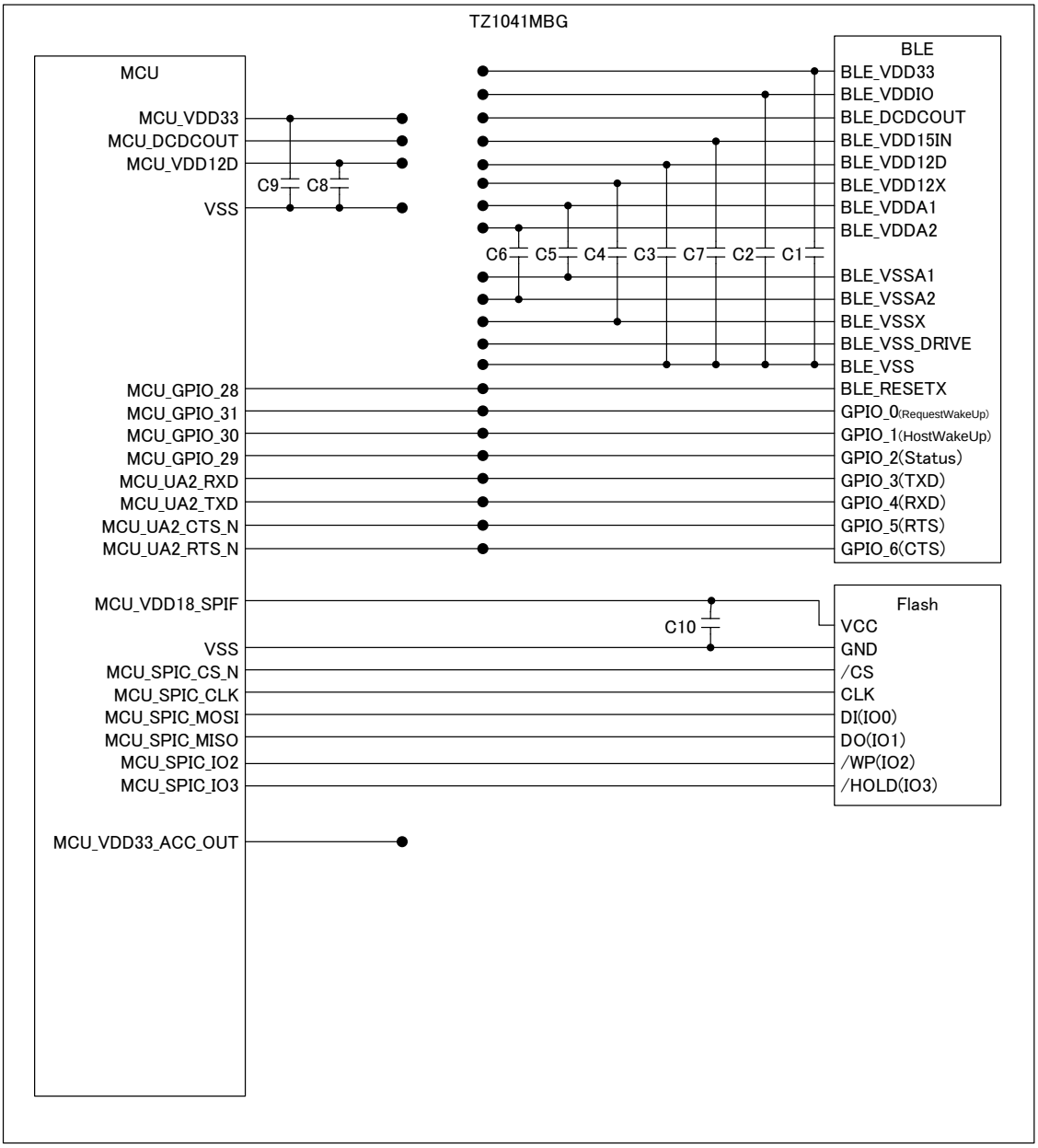


Figure 5.2 Internal connection of each signal in TZ1041MBG

(The large "●" means a connection with external pin of the TZ1041MBG.)

The list of internal capacitance value in the TZ1041MBG package is shown in "Table 5.1 Internal capacitor in TZ1041MBG."

Table 5.1 Internal capacitor in TZ1041MBG

Capacitance		Internal connection	
1 μF	C1	BLE_VDD33	BLE_VSS
	C2	BLE_VDDIO	BLE_VSS
	C7	BLE_VDD15IN	BLE_VSS
	C8	MCU_VDD12D	VSS
	C9	MCU_VDD33	VSS
	C10	MCU_VDD18_SPIF_OUT	VSS
0.1 μF	C3	BLE_VDD12D	BLE_VSS
	C4	BLE_VDD12X	BLE_VSSX
	C5	BLE_VDD12A1	BLE_VSSA1
	C6	BLE_VDD12A2	BLE_VSSA2

5.2. Pin alignment (TOP View)

TOPVIEW

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	MCU_GPIO_14		MCU_I2C1_DATA	BLE_VSS	BLE_VSSA1	BLE_VSSA2	BLE_RFIOP	BLE_RFION	BLE_VSSA2	BLE_VDD12X	BLE_VSS	A
B	MCU_UA1_RXD	MCU_GPIO_15	MCU_UA1_RTS_N	MCU_I2C1_CLK	BLE_VPGM	BLE_VSS	BLE_VDD12A1	BLE_VSSA2	BLE_VSSA2	BLE_VDD12A2	BLE_VSSX	BLE_XOOUT	B
C	MCU_UA1_TXD	MCU_GPIO_13	MCU_UA1_CTS_N	BLE_GPIO7	BLE_AMONITOR1	BLE_AMONITOR2	BLE_VSS			BLE_VSS	BLE_DCDCEN	BLE_XOIN	C
D		MCU_GPIO_12	MCU_VDD33_ACC_OUT		BLE_GPIO12	BLE_GPIO13	BLE_GPIO8			BLE_VDDIO	BLE_VSS_DRIVE	BLE_VSS	D
E	MCU_GPIO_10	MCU_GPIO_11	MCU_VDD18_SPIF_OUT		BLE_GPIO10	BLE_GPIO11	BLE_GPIO9		BLE_GPIO4	BLE_VDD33	BLE_VDD12D	BLE_VDD15IN	E
F	MCU_GPIO_9	MCU_TEST	VSS			BLE_GPIO6	BLE_GPIO5		BLE_GPIO3	BLE_GPIO15	BLE_GPIO14	BLE_DCDCOUT	F
G	MCU_GPIO_7	MCU_GPIO_8	VSS	MCU_BOOTMODE3					BLE_TMODE2	BLE_RESETX	BLE_GPIO0	BLE_SLPXOOUT	G
H		MCU_GPIO_6	MCU_UA0_RXD	MCU_BOOTMODE2					BLE_TMODE1	BLE_GPIO2	BLE_GPIO1	BLE_SLPXOIN	H
J	MCU_GPIO_5	MCU_GPIO_4	MCU_UA0_TXD	MCU_BOOTMODE1					VSS	MCU_VPGM	MCU_BGR_OUT	MCU_CLK32K_OUT	J
K	MCU_GPIO_3	MCU_GPIO_2	MCU_I2C0_DATA	MCU_BOOTMODE0							VSS	MCU_BOOTMODE4	K
L		MCU_GPIO_1	MCU_I2C0_CLK	VSS					MCU_ADC_AIN0		MCU_SYS_RESET_N		L
M	MCU_GPIO_0	MCU_VDD33_MAG_OUT	MCU_VDD33_GYRO_OUT	MCU_DBG_TDO	MCU_ADC24_SYNC		MCU_VREFH_ADC12	MCU_VREFL_ADC12	MCU_VREFL_ADC24	MCU_AVDD33_ADC	MCU_VDD12D	MCU_DCDCOUT	M
N	MCU_SPIM1_MISO	MCU_DBG_TRST_N	MCU_DBG_TDI	MCU_SPIM0_CS_N	MCU_DBG_TCK	MCU_DBG_TMS	MCU_VDD33_USB	MCU_VSS_USB	MCU_AVSS_ADC	MCU_VREFH_ADC24	MCU_VDD33	MCU_XIN_32K	N
P	MCU_SPIM1_MOSI	MCU_SPIM1_CS_N	MCU_SPIM0_MISO	MCU_SPIM0_MOSI		MCU_USB_DP	MCU_VDD33_USB_OUT	MCU_ADC_AIN1	MCU_ADC_AIN3	MCU_ADC_AIN5	MCU_XIN_12M	MCU_XOUT_32K	P
R	VSS	MCU_SPIM1_CLK		MCU_SPIM0_CLK		MCU_USB_DM		MCU_ADC_AIN2	MCU_ADC_AIN4		MCU_XOUT_12M	VSS	R
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 5.3 Pin alignments on TZ1041MBG package (Top View)

5.3. Pin assignment table

Table 5.2 Pin assignment table

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1	VSS	E10	BLE_VDD33	M3	MCU_VDD33_GYRO_OUT
A2	MCU_GPIO_14	E11	BLE_VDD12D	M4	MCU_DBG_TDO
A4	MCU_I2C1_DATA	E12	BLE_VDD15IN	M5	MCU_ADC24_SYNC
A5	BLE_VSS	F1	MCU_GPIO_9	M7	MCU_VREFH_ADC12
A6	BLE_VSSA1	F2	MCU_TEST	M8	MCU_VREFL_ADC12
A7	BLE_VSSA2	F3	VSS	M9	MCU_VREFL_ADC24
A8	BLE_RFIOP	F6	BLE_GPIO6	M10	MCU_AVDD33_ADC
A9	BLE_RFION	F7	BLE_GPIO5	M11	MCU_VDD12D
A10	BLE_VSSA2	F9	BLE_GPIO3	M12	MCU_DCDCOUT
A11	BLE_VDD12X	F10	BLE_GPIO15	N1	MCU_SPIM1_MISO
A12	BLE_VSS	F11	BLE_GPIO14	N2	MCU_DBG_TRST_N
B1	MCU_UA1_RXD	F12	BLE_DCDCOUT	N3	MCU_DBG_TDI
B2	MCU_GPIO_15	G1	MCU_GPIO_7	N4	MCU_SPIM0_CS_N
B3	MCU_UA1_RTS_N	G2	MCU_GPIO_8	N5	MCU_DBG_TCK
B4	MCU_I2C1_CLK	G3	VSS	N6	MCU_DBG_TMS
B5	BLE_VPGM	G4	MCU_BOOTMODE3	N7	MCU_VDD33_USB
B6	BLE_VSS	G9	BLE_TMODE2	N8	MCU_VSS_USB
B7	BLE_VDD12A1	G10	BLE_RESETX	N9	MCU_AVSS_ADC
B8	BLE_VSSA2	G11	BLE_GPIO0	N10	MCU_VREFH_ADC24
B9	BLE_VSSA2	G12	BLE_SLPXOOUT	N11	MCU_VDD33
B10	BLE_VDD12A2	H2	MCU_GPIO_6	N12	MCU_XIN_32K
B11	BLE_VSSX	H3	MCU_UA0_RXD	P1	MCU_SPIM1_MOSI
B12	BLE_XOOUT	H4	MCU_BOOTMODE2	P2	MCU_SPIM1_CS_N
C1	MCU_UA1_TXD	H9	BLE_TMODE1	P3	MCU_SPIM0_MISO
C2	MCU_GPIO_13	H10	BLE_GPIO2	P4	MCU_SPIM0_MOSI
C3	MCU_UA1_CTS_N	H11	BLE_GPIO1	P6	MCU_USB_DP
C4	BLE_GPIO7	H12	BLE_SLPXOIN	P7	MCU_VDD33_USB_OUT
C5	BLE_AMONITOR1	J1	MCU_GPIO_5	P8	MCU_ADC_AIN1
C6	BLE_AMONITOR2	J2	MCU_GPIO_4	P9	MCU_ADC_AIN3
C7	BLE_VSS	J3	MCU_UA0_TXD	P10	MCU_ADC_AIN5
C10	BLE_VSS	J4	MCU_BOOTMODE1	P11	MCU_XIN_12M
C11	BLE_DCDCEN	J9	VSS	P12	MCU_XOUT_32K
C12	BLE_XOIN	J10	MCU_VPGM	R1	VSS
D2	MCU_GPIO_12	J11	MCU_BGR_OUT	R2	MCU_SPIM1_CLK
D3	MCU_VDD33_ACC_OUT	J12	MCU_CLK32K_OUT	R4	MCU_SPIM0_CLK
D5	BLE_GPIO12	K1	MCU_GPIO_3	R6	MCU_USB_DM
D6	BLE_GPIO13	K2	MCU_GPIO_2	R8	MCU_ADC_AIN2
D7	BLE_GPIO8	K3	MCU_I2C0_DATA	R9	MCU_ADC_AIN4
D10	BLE_VDDIO	K4	MCU_BOOTMODE0	R11	MCU_XOUT_12M
D11	BLE_VSS_DRIVE	K11	VSS	R12	VSS
D12	BLE_VSS	K12	MCU_BOOTMODE4		
E1	MCU_GPIO_10	L2	MCU_GPIO_1		
E2	MCU_GPIO_11	L3	MCU_I2C0_CLK		
E3	MCU_VDD18_SPIF_OUT	L4	VSS		
E5	BLE_GPIO10	L9	MCU_ADC_AIN0		
E6	BLE_GPIO11	L11	MCU_SYS_RESET_N		
E7	BLE_GPIO9	M1	MCU_GPIO_0		
E9	BLE_GPIO4	M2	MCU_VDD33_MAG_OUT		

6. Terminal description

Terminal attribute shows that the grouping of the terminals classified by their structures and power type.

Table 6.1 Terminal Attribute

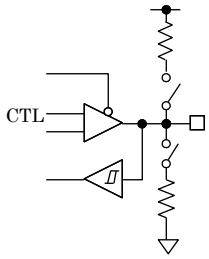
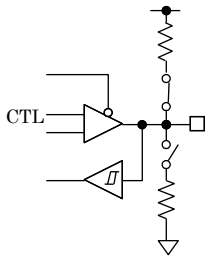
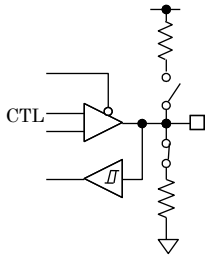
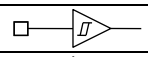
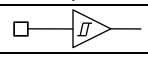
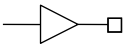
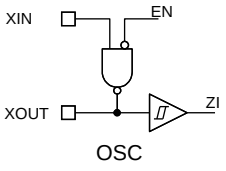
Attribute	Explanation	Structure
BDSPZ	Bi-directional buffer, 2/4/5/7 mA drive, Schmitt trigger LVCMOS level input with programmable pull-up and pull-down resistors. Supply voltage of pull-up resistor is VDD33.	
BDSPU	Bi-directional buffer, 2/4/5/7 mA drive, Schmitt trigger LVCMOS level input with programmable pull-up and pull-down resistors. (By default, pull-up resistor is ON) Supply voltage of pull-up resistor is VDD33.	
BDSPD	Bi-directional buffer, 2/4/5/7 mA drive, Schmitt trigger LVCMOS level input with programmable pull-up and pull-down resistors. (By default, pull-down resistor is ON) Supply voltage of pull-up resistor is VDD33.	
IS	Schmitt Trigger LVCMOS Input Buffer	
IS5	Schmitt Trigger, 5 V Tolerant LVCMOS Input Buffer	
O2	Output Buffer, 2 mA Output	
OSC	Oscillator buffer	
USB-IO	Receiving and transporting for USB differential data	—
POWER	Digital power supply	—
GND	Digital GND	—
ANALOG	Analog signal	—
A-POWER	Analog power supply	—
A-GND	Analog GND	—
OTHER	Other terminal with structures other than above	—

Table 6.2 TZ1041MBG Terminal

Ball number	Terminal name	Attribute	I/O	Explanation
N12	MCU_XIN_32K	OSC	In	Oscillator input for RTC clock (32.768 kHz)
P12	MCU_XOUT_32K	OSC	Out	Oscillator output for RTC clock (32.768 kHz)
P11	MCU_XIN_12M	OSC	In	Oscillator input for System clock (12 MHz)
R11	MCU_XOUT_12M	OSC	Out	Oscillator output for System clock (12 MHz)
J12	MCU_CLK32K_OUT	O2	Out	Clock for BLE RTC clock supply (32.768 kHz)
L11	MCU_SYS_RESET_N	IS	In	System reset input
K4	MCU_BOOTMODE0	IS	In	Boot mode select 0
J4	MCU_BOOTMODE1	IS	In	Boot mode select 1
H4	MCU_BOOTMODE2	IS	In	Boot mode select 2
G4	MCU_BOOTMODE3	IS	In	Boot mode select 3
K12	MCU_BOOTMODE4	IS	In	Boot mode select 4
N5	MCU_DBG_TCK	BDSPD	In	ARM core Debug clock input (TCK) / SWD clock input (SWCLK)
M4	MCU_DBG_TDO	BDSPZ	Out	ARM core Debug data output (TDO) / SWV trace data output (SWO)
N3	MCU_DBG_TDI	BDSPU	In	ARM core Debug data input (TDI)
N6	MCU_DBG_TMS	BDSPU	IO	ARM core Debug mode select (TMS) / SWD data in/out (SWDIO)
N2	MCU_DBG_TRST_N	BDSPU	In	ARM core Debug reset input (TRST_N)
P6	MCU_USB_DP	USB-IO	IO	USB differential signal pair [positive/negative]
R6	MCU_USB_DM	USB-IO	IO	
M1	MCU_GPIO_0	IS5	In	Multiple function I/O (GPIO_0)
L2	MCU_GPIO_1	BDSPZ	IO	Multiple function I/O (GPIO_1)
K2	MCU_GPIO_2	BDSPZ	IO	Multiple function I/O (GPIO_2)
K1	MCU_GPIO_3	BDSPZ	IO	Multiple function I/O (GPIO_3)
J2	MCU_GPIO_4	BDSPZ	IO	Multiple function I/O (GPIO_4)
J1	MCU_GPIO_5	BDSPZ	IO	Multiple function I/O (GPIO_5)
H2	MCU_GPIO_6	BDSPZ	IO	Multiple function I/O (GPIO_6)
G1	MCU_GPIO_7	BDSPZ	IO	Multiple function I/O (GPIO_7)
G2	MCU_GPIO_8	BDSPZ	IO	Multiple function I/O (GPIO_8 / PWM0 / TRACEDATA[0])
F1	MCU_GPIO_9	BDSPZ	IO	Multiple function I/O (GPIO_9 / PWM1 / TRACEDATA[1])
E1	MCU_GPIO_10	BDSPZ	IO	Multiple function I/O (GPIO_10 / PWM2 / TRACEDATA[2])
E2	MCU_GPIO_11	BDSPZ	IO	Multiple function I/O (GPIO_11 / PWM3 / TRACEDATA[3])
D2	MCU_GPIO_12	BDSPZ	IO	Multiple function I/O (GPIO_12 / SPIM3_CS_N / CAPTURE0)
C2	MCU_GPIO_13	BDSPZ	IO	Multiple function I/O (GPIO_13 / SPIM3_CLK / CAPTURE1)
A2	MCU_GPIO_14	BDSPZ	IO	Multiple function I/O (GPIO_14 / SPIM3_MOSI / UA0_RTS_N)
B2	MCU_GPIO_15	BDSPZ	IO	Multiple function I/O (GPIO_15 / SPIM3_MISO / UA0_CTS_N)

Ball number	Terminal name	Attribute	I/O	Explanation
K3	MCU_I2C0_DATA	BDSPZ	IO	Multiple function I/O (I2C0_DATA / CAPTURE2 / GPIO_16)
L3	MCU_I2C0_CLK	BDSPZ	IO	Multiple function I/O (I2C0_CLK / CAPTURE3 / GPIO_17)
A4	MCU_I2C1_DATA	BDSPZ	IO	Multiple function I/O (I2C1_DATA / UA0_RTS_N / GPIO_14)
B4	MCU_I2C1_CLK	BDSPZ	IO	Multiple function I/O (I2C1_CLK / UA0_CTS_N / GPIO_15)
H3	MCU_UA0_RXD	BDSPZ	IO	Multiple function I/O (UA0_RXD / CAPTURE0 / GPIO_20)
J3	MCU_UA0_TXD	BDSPZ	IO	Multiple function I/O (UA0_TXD / CAPTURE1 / GPIO_21)
B1	MCU_UA1_RXD	BDSPZ	IO	Multiple function I/O (UA1_RXD / I2C0_CLK / GPIO_12)
C1	MCU_UA1_TXD	BDSPZ	IO	Multiple function I/O (UA1_TXD / I2C0_DATA / GPIO_13)
B3	MCU_UA1_RTS_N	BDSPZ	IO	Multiple function I/O (UA1_RTS_N / I2C2_DATA / GPIO_22)
C3	MCU_UA1_CTS_N	BDSPZ	IO	Multiple function I/O (UA1_CTS_N / I2C2_CLK / GPIO_23)
N4	MCU_SPIM0_CS_N	BDSPZ	IO	Multiple function I/O (SPIM0_CS_N / GPIO_16 / PWM0)
R4	MCU_SPIM0_CLK	BDSPZ	IO	Multiple function I/O (SPIM0_CLK / GPIO_17 / PWM1)
P4	MCU_SPIM0_MOSI	BDSPZ	IO	Multiple function I/O (SPIM0_MOSI / GPIO_18 / PWM2)
P3	MCU_SPIM0_MISO	BDSPZ	IO	Multiple function I/O (SPIM0_MISO / GPIO_19 / TRACECLK)
P2	MCU_SPIM1_CS_N	BDSPZ	IO	Multiple function I/O (SPIM1_CS_N / GPIO_20 / UA0_RXD)
R2	MCU_SPIM1_CLK	BDSPZ	IO	Multiple function I/O (SPIM1_CLK / GPIO_21 / UA0_TXD)
P1	MCU_SPIM1_MOSI	BDSPZ	IO	Multiple function I/O (SPIM1_MOSI / GPIO_22)
N1	MCU_SPIM1_MISO	BDSPZ	IO	Multiple function I/O (SPIM1_MISO / GPIO_23)
M5	MCU_ADC24_SYNC	BDSPZ	IO	Multiple function I/O (ADC24_SYNC / GPIO_8)
L9	MCU_ADC_AIN0	ANALOG	In	ADC12 channel0 or ADC24 channel0 +
P8	MCU_ADC_AIN1	ANALOG	In	ADC12 channel1 or ADC24 channel0 -
R8	MCU_ADC_AIN2	ANALOG	In	ADC12 channel2 or ADC24 channel1 +
P9	MCU_ADC_AIN3	ANALOG	In	ADC12 channel3 or ADC24 channel1 -
R9	MCU_ADC_AIN4	ANALOG	In	ADC24 channel2 +
P10	MCU_ADC_AIN5	ANALOG	In	ADC24 channel2 -
M7	MCU_VREFH_ADC12	ANALOG	In	ADC12 VREFH
N10	MCU_VREFH_ADC24	ANALOG	In	ADC24 VREFH
M8	MCU_VREFL_ADC12	ANALOG	In	ADC12 VREFL
M9	MCU_VREFL_ADC24	ANALOG	In	ADC24 VREFL
J10	MCU_VPGM	OTHER	In	For test, Connect to VSS.
F2	MCU_TEST	IS	In	For test, Connect to VSS.
J11	MCU_BGR_OUT	ANALOG	Out	BGR Monitor output
M2	MCU_VDD33_MAG_OUT	ANALOG	—	Voltage Monitor pin. It cannot be used as a power supply for other devices.

Ball number	Terminal name	Attribute	I/O	Explanation
D3	MCU_VDD33_ACC_OUT	ANALOG	—	Voltage Monitor pin. It cannot be used as a power supply for other devices.
M3	MCU_VDD33_GYRO_OUT	ANALOG	—	Voltage Monitor pin. It cannot be used as a power supply for other devices.
E3	MCU_VDD18_SPIF_OUT	ANALOG	—	Voltage Monitor pin for power of the internal SPI Flash memory and SPIC I/Os. The bypass capacitor connection point for built-in Flash power line. (Add 10 µF capacitor with X5R characteristic between this pin and VSS on the board.) It cannot be used as a power supply for other devices.
N11	MCU_VDD33	POWER	—	VDD input
M12	MCU_DCDCOUT	POWER	—	DCDC output
M11	MCU_VDD12D	POWER	—	Digital 1.2 V input
N7	MCU_VDD33_USB	POWER	—	USB IO Power
N8	MCU_VSS_USB	GND	—	USB GND
P7	MCU_VDD33_USB_OUT	POWER	—	Power pin for the pull-up resistance of the USB device signal. It cannot be used as a power supply for other devices.
M10	MCU_AVDD33_ADC	A-POWER	—	ADC IO Power
N9	MCU_AVSS_ADC	A-GND	—	ADC analog GND
A1, F3, G3, J9, K11, L4, R1, R12	VSS	GND	—	GND
G10	BLE_RESETX	IS	In	BLE reset input Internally connected to MCU_GPIO_28. (Refer to Figure 5.2)
C11	BLE_DCDCEN	IS	In	BLE DCDC enable
C12	BLE_XOIN	OTHER	In	Oscillator or TCXO input pin for Baseband and RF reference clock (26 MHz).
B12	BLE_XOOUT	OTHER	Out	
H12	BLE_SLPXOIN	OSC	In	Oscillator input for BLE RTC clock (32.768 kHz)
G12	BLE_SLPXOOUT	OSC	Out	Oscillator output for BLE RTC clock (32.768 kHz)
A8	BLE_RFIOP	OTHER	IO	Bluetooth RF differential I/O
A9	BLE_RFION	OTHER	IO	
G11	BLE_GPIO0	BDSPZ	IO	BLE GPIO0 / RequestWakeUp Internally connected to MCU_GPIO_31. (Refer to Figure 5.2)
H11	BLE_GPIO1	BDSPZ	IO	BLE GPIO1 / HostWakeUp Internally connected to MCU_GPIO_30. (Refer to Figure 5.2)
H10	BLE_GPIO2	BDSPZ	IO	BLE GPIO2 / Status Internally connected to MCU_GPIO_29. (Refer to Figure 5.2)
F9	BLE_GPIO3	BDSPU	IO	BLE GPIO3 / UART1-TX Internally connected to MCU_UA2_RXD. (Refer to Figure 5.2)
E9	BLE_GPIO4	BDSPU	IO	BLE GPIO4 / UART1-RX Internally connected to MCU_UA2_TXD. (Refer to Figure 5.2)

Ball number	Terminal name	Attribute	I/O	Explanation
F7	BLE_GPIO5	BDSPU	IO	BLE GPIO5 / UART1-RTSX Internally connected to MCU_UA2_CTS_N. (Refer to Figure 5.2)
F6	BLE_GPIO6	BDSPU	IO	BLE GPIO6 / UART1-CTSX Internally connected to MCU_UA2_RTS_N. (Refer to Figure 5.2)
C4	BLE_GPIO7	BDSPU	IO	For test, Leave this ball open.
D7	BLE_GPIO8	BDSPU	IO	For test, Leave this ball open.
E7	BLE_GPIO9	BDSPU	IO	For test, Leave this ball open.
E5	BLE_GPIO10	BDSPU	IO	For test, Leave this ball open.
E6	BLE_GPIO11	BDSPU	IO	For test, Leave this ball open.
D5	BLE_GPIO12	BDSPU	IO	For test, Leave this ball open.
D6	BLE_GPIO13	BDSPU	IO	For test, Leave this ball open.
F11	BLE_GPIO14	BDSPU	IO	For test, Leave this ball open.
F10	BLE_GPIO15	BDSPZ	IO	For test, Leave this ball open.
H9	BLE_TMODE1	IS	In	For test, Connect to BLE_VSS.
G9	BLE_TMODE2	IS	In	For test, Connect to BLE_VSS.
C5	BLE_AMONITOR1	OTHER	IO	For test, Connect to BLE_VSS.
C6	BLE_AMONITOR2	OTHER	IO	For test, Connect to BLE_VSS.
B5	BLE_VPGM	OTHER	In	For test, Connect to BLE_VSS.
E10	BLE_VDD33	POWER	—	Power supply for DCDC and sleep circuit.
D10	BLE_VDDIO	POWER	—	Power supply for IO of BLE chip.
F12	BLE_DCDCOUT	POWER	—	DCDC output
E12	BLE_VDD15IN	POWER	—	Power supply for internal regulator.
B7	BLE_VDD12A1	A-POWER	—	Power supply for Analog circuit (1.2 V)
E11	BLE_VDD12D	POWER	—	Power supply for Digital circuit (1.2 V)
A11	BLE_VDD12X	A-POWER	—	Power supply for OSC (1.2 V)
B10	BLE_VDD12A2	A-POWER	—	Power supply for Analog circuit (1.2 V)
A6	BLE_VSSA1	A-GND	—	Analog GND
A7, A10, B8, B9	BLE_VSSA2	A-GND	—	Analog GND
B11	BLE_VSSX	A-GND	—	GND for OSC
D11	BLE_VSS_DRIVE	GND	—	GND for DCDC
A5, A12, B6, C7, C10, D12	BLE_VSS	GND	—	GND

Please refer to the BLE chip's datasheet for the details of the BLE_* terminals.

6.1. Setting Multiple function I/O

Some of terminals have multiple functions with this product. A register setup defines or changes a function of the terminal after booting up this product.

After booting up, terminal functions are defined with ***[FMODE_CFGn]*** registers in the GCONF module as follows.

Table 6.3 *[FMODE_CFGn]* Register Address

Control register	Address
FMODE_CFG0	0x4004_A140
FMODE_CFG1	0x4004_A144
FMODE_CFG2	0x4004_A148
FMODE_CFG3	0x4004_A14C
FMODE_CFG4	0x4004_A150
FMODE_CFG5	0x4004_A154
FMODE_CFG6	0x4004_A158

The following table describes terminal functions defined with each bit of ***[FMODE_CFGn]***.TERM_NAME_FMODE[1:0].

Table 6.4 Multiple function I/O

Ball	Terminal name	Control register	Function name			
			***[FMODE_CFGn]*.TERM_NAME_FMODE[1:0]**			
			0b00	**0b01**	**0b10**	**0b11**
			Mode0 (Initial)	**Mode1 (Main)**	**Mode2 (Alternate)**	**Mode3 (Alternate)**
M1	MCU_GPIO_0	***[FMODE_CFG0]***. GPIO_0_FMODE	No Function	GPIO_0	No Function	No Function
L2	MCU_GPIO_1	***[FMODE_CFG0]***. GPIO_1_FMODE	No Function	GPIO_1	No Function	No Function
K2	MCU_GPIO_2	***[FMODE_CFG0]***. GPIO_2_FMODE	No Function	GPIO_2	No Function	No Function
K1	MCU_GPIO_3	***[FMODE_CFG0]***. GPIO_3_FMODE	No Function	GPIO_3	No Function	No Function
J2	MCU_GPIO_4	***[FMODE_CFG0]***. GPIO_4_FMODE	No Function	GPIO_4	No Function	No Function
J1	MCU_GPIO_5	***[FMODE_CFG0]***. GPIO_5_FMODE	No Function	GPIO_5	No Function	No Function
H2	MCU_GPIO_6	***[FMODE_CFG0]***. GPIO_6_FMODE	No Function	GPIO_6	No Function	No Function
G1	MCU_GPIO_7	***[FMODE_CFG0]***. GPIO_7_FMODE	No Function	GPIO_7	No Function	No Function
G2	MCU_GPIO_8	***[FMODE_CFG0]***. GPIO_8_FMODE	No Function	GPIO_8	PWM0	TRACEDATA[0]
F1	MCU_GPIO_9	***[FMODE_CFG0]***. GPIO_9_FMODE	No Function	GPIO_9	PWM1	TRACEDATA[1]
E1	MCU_GPIO_10	***[FMODE_CFG0]***. GPIO_10_FMODE	No Function	GPIO_10	PWM2	TRACEDATA[2]
E2	MCU_GPIO_11	***[FMODE_CFG0]***. GPIO_11_FMODE	No Function	GPIO_11	PWM3	TRACEDATA[3]
D2	MCU_GPIO_12	***[FMODE_CFG0]***. GPIO_12_FMODE	No Function	GPIO_12	SPIM3_CS_N	CAPTURE0
C2	MCU_GPIO_13	***[FMODE_CFG0]***. GPIO_13_FMODE	No Function	GPIO_13	SPIM3_CLK	CAPTURE1
A2	MCU_GPIO_14	***[FMODE_CFG0]***. GPIO_14_FMODE	No Function	GPIO_14	SPIM3_MOSI	UA0_RTS_N
B2	MCU_GPIO_15	***[FMODE_CFG0]***. GPIO_15_FMODE	No Function	GPIO_15	SPIM3_MISO	UA0_CTS_N
—	MCU_GPIO_24	***[FMODE_CFG1]***. GPIO_24_FMODE	No Function	GPIO_24	No Function	No Function

Ball	Terminal name	Control register	Function name			
			[FMODE_CFGn].TERM_NAME_FMODE[1:0]			
			0b00	0b01	0b10	0b11
			Mode0 (Initial)	Mode1 (Main)	Mode2 (Alternate)	Mode3 (Alternate)
—	MCU_GPIO_25	***[FMODE_CFG1]***. GPIO_25_FMODE	No Function	GPIO_25	No Function	No Function
—	MCU_GPIO_26	***[FMODE_CFG1]***. GPIO_26_FMODE	No Function	GPIO_26	No Function	No Function
—	MCU_GPIO_27	***[FMODE_CFG1]***. GPIO_27_FMODE	No Function	GPIO_27	No Function	PWM3
(G10)	MCU_GPIO_28	***[FMODE_CFG1]***. GPIO_28_FMODE	No Function	GPIO_28	No Function	No Function
(H10)	MCU_GPIO_29	***[FMODE_CFG1]***. GPIO_29_FMODE	No Function	GPIO_29	No Function	No Function
(H11)	MCU_GPIO_30	***[FMODE_CFG1]***. GPIO_30_FMODE	No Function	GPIO_30	No Function	No Function
(G11)	MCU_GPIO_31	***[FMODE_CFG1]***. GPIO_31_FMODE	No Function	GPIO_31	No Function	No Function
K3	MCU_I2C0_DATA	***[FMODE_CFG2]***. I2C0_DATA_FMODE	No Function	I2C0_DATA (Note1)	CAPTURE2	GPIO_16
L3	MCU_I2C0_CLK	***[FMODE_CFG2]***. I2C0_CLK_FMODE	No Function	I2C0_CLK (Note1)	CAPTURE3	GPIO_17
A4	MCU_I2C1_DATA	***[FMODE_CFG2]***. I2C1_DATA_FMODE	No Function	I2C1_DATA (Note1)	UA0_RTS_N	GPIO_14
B4	MCU_I2C1_CLK	***[FMODE_CFG2]***. I2C1_CLK_FMODE	No Function	I2C1_CLK (Note1)	UA0_CTS_N	GPIO_15
—	MCU_I2C2_DATA	***[FMODE_CFG2]***. I2C2_FMODE	No Function	I2C2_DATA (Note1)	No Function	No Function
—	MCU_I2C2_CLK		No Function	I2C2_CLK (Note1)	No Function	No Function
H3	MCU_UA0_RXD	***[FMODE_CFG3]***. UA0_RXD_FMODE	No Function	UA0_RXD	CAPTURE0	GPIO_20
J3	MCU_UA0_TXD	***[FMODE_CFG3]***. UA0_TXD_FMODE	No Function	UA0_TXD	CAPTURE1	GPIO_21
B1	MCU_UA1_RXD	***[FMODE_CFG3]***. UA1_RXD_FMODE	No Function	UA1_RXD	I2C0_CLK (Note1)	GPIO_12
C1	MCU_UA1_TXD	***[FMODE_CFG3]***. UA1_TXD_FMODE	No Function	UA1_TXD	I2C0_DATA (Note1)	GPIO_13
B3	MCU_UA1_RTS_N	***[FMODE_CFG3]***. UA1_RTS_N_FMODE	No Function	UA1_RTS_N	I2C2_DATA (Note1)	GPIO_22
C3	MCU_UA1_CTS_N	***[FMODE_CFG3]***. UA1_CTS_N_FMODE	No Function	UA1_CTS_N	I2C2_CLK (Note1)	GPIO_23
(F9)	MCU_UA2_RXD	***[FMODE_CFG3]***. UA2_RXD_FMODE	No Function	UA2_RXD	No Function	GPIO_18
(E9)	MCU_UA2_TXD	***[FMODE_CFG3]***. UA2_TXD_FMODE	No Function	UA2_TXD	No Function	GPIO_19
(F6)	MCU_UA2_RTS_N	***[FMODE_CFG3]***. UA2_RTS_N_FMODE	No Function	UA2_RTS_N	No Function	GPIO_10
(F7)	MCU_UA2_CTS_N	***[FMODE_CFG3]***. UA2_CTS_N_FMODE	No Function	UA2_CTS_N	No Function	GPIO_11
N4	MCU_SPIM0_CS_N	***[FMODE_CFG4]***. SPIM0_CS_N_FMODE	No Function	SPIM0_CS_N	GPIO_16	PWM0
R4	MCU_SPIM0_CLK	***[FMODE_CFG4]***. SPIM0_ CLK_FMODE	No Function	SPIM0_CLK	GPIO_17	PWM1
P4	MCU_SPIM0_MOSI	***[FMODE_CFG4]***. SPIM0_MOSI_FMODE	No Function	SPIM0_MOSI	GPIO_18	PWM2
P3	MCU_SPIM0_MISO	***[FMODE_CFG4]***. SPIM0_MISO_FMODE	No Function	SPIM0_MISO	GPIO_19	TRACECLK
P2	MCU_SPIM1_CS_N	***[FMODE_CFG4]***. SPIM1_CS_N_FMODE	No Function	SPIM1_CS_N	GPIO_20	UA0_RXD
R2	MCU_SPIM1_CLK	***[FMODE_CFG4]***. SPIM1_CLK_FMODE	No Function	SPIM1_CLK	GPIO_21	UA0_TXD
P1	MCU_SPIM1_MOSI	***[FMODE_CFG4]***. SPIM1_MOSI_FMODE	No Function	SPIM1_MOSI	GPIO_22	No Function

Ball	Terminal name	Control register	Function name			
			[FMODE_CFGn].TERM_NAME_FMODE[1:0]			
			0b00	0b01	0b10	0b11
			Mode0 (Initial)	Mode1 (Main)	Mode2 (Alternate)	Mode3 (Alternate)
N1	MCU_SPIM1_MISO	***[FMODE_CFG4]***. SPIM1_MISO_FMODE	No Function	SPIM1_MISO	GPIO_23	No Function
—	MCU_SPIM2_CS_N	***[FMODE_CFG4]***. SPIM2_FMODE	No Function	SPIM2_CS_N	No Function	No Function
—	MCU_SPIM2_CLK		No Function	SPIM2_CLK	No Function	No Function
—	MCU_SPIM2_MOSI		No Function	SPIM2_MOSI	No Function	No Function
—	MCU_SPIM2_MISO		No Function	SPIM2_MISO	No Function	No Function
—	MCU_SPIM3_CS_N	***[FMODE_CFG4]***. SPIM3_FMODE	No Function	SPIM3_CS_N	No Function	No Function
—	MCU_SPIM3_CLK		No Function	SPIM3_CLK	No Function	No Function
—	MCU_SPIM3_MOSI		No Function	SPIM3_MOSI	No Function	No Function
—	MCU_SPIM3_MISO		No Function	SPIM3_MISO	No Function	No Function
—	MCU_SPIC_CS_N	***[FMODE_CFG5]***. SPIC_FMODE	SPIC_CS_N	No Function	SPIC_CS_N	SPIC_CS_N
—	MCU_SPIC_CLK		SPIC_CLK	No Function	SPIC_CLK	SPIC_CLK
—	MCU_SPIC_MOSI		SPIC_MOSI	No Function	SPIC_MOSI	SPIC_MOSI
—	MCU_SPIC_MISO		SPIC_MISO	No Function	SPIC_MISO	SPIC_MISO
—	MCU_SPIC_IO2		SPIC_IO2	No Function	SPIC_IO2	SPIC_IO2
—	MCU_SPIC_IO3		SPIC_IO3	No Function	SPIC_IO3	SPIC_IO3
M5	MCU_ADC24_SYNC	***[FMODE_CFG6]***. ADC24_SYNC_FMODE	No Function	ADC24_SYNC	No Function	GPIO_8

Note: It forbids assigning the same function simultaneously to two or more terminals.

Note1: Terminal is set to a pseudo open drain.

Table 6.5 Function name

Function name	I/O	Explanation
No Function	In	"No function" indicates a state in which the terminal is not connected to any controller. (Open inside the chip)
GPIO		
GPIO_0	In	Programmable I/O 0: GPIO0 PIN0 (Can be used for USB VBUS detection, Wakeup, Input Only)
GPIO_1	IO	Programmable I/O 1: GPIO0 PIN1 (Can be used for Wakeup)
GPIO_2	IO	Programmable I/O 2: GPIO0 PIN2 (Can be used for Wakeup)
GPIO_3	IO	Programmable I/O 3: GPIO0 PIN3 (Can be used for Wakeup)
GPIO_4	IO	Programmable I/O 4: GPIO0 PIN4 (Can be used for Wakeup)
GPIO_5	IO	Programmable I/O 5: GPIO0 PIN5 (Can be used for Wakeup)
GPIO_6	IO	Programmable I/O 6: GPIO0 PIN6 (Can be used for Wakeup)
GPIO_7	IO	Programmable I/O 7: GPIO0 PIN7 (Can be used for Wakeup)
GPIO_8	IO	Programmable I/O 8: GPIO1 PIN0
GPIO_9	IO	Programmable I/O 9: GPIO1 PIN1
GPIO_10	IO	Programmable I/O 10: GPIO1 PIN2
GPIO_11	IO	Programmable I/O 11: GPIO1 PIN3
GPIO_12	IO	Programmable I/O 12: GPIO1 PIN4
GPIO_13	IO	Programmable I/O 13: GPIO1 PIN5
GPIO_14	IO	Programmable I/O 14: GPIO1 PIN6
GPIO_15	IO	Programmable I/O 15: GPIO1 PIN7

Function name	I/O	Explanation
GPIO_16	IO	Programmable I/O 16: GPIO2 PIN0
GPIO_17	IO	Programmable I/O 17: GPIO2 PIN1
GPIO_18	IO	Programmable I/O 18: GPIO2 PIN2
GPIO_19	IO	Programmable I/O 19: GPIO2 PIN3
GPIO_20	IO	Programmable I/O 20: GPIO2 PIN4
GPIO_21	IO	Programmable I/O 21: GPIO2 PIN5
GPIO_22	IO	Programmable I/O 22: GPIO2 PIN6
GPIO_23	IO	Programmable I/O 23: GPIO2 PIN7
GPIO_24	IO	Programmable I/O 24: GPIO3 PIN0 (Can be used for Wakeup)
GPIO_25	IO	Programmable I/O 25: GPIO3 PIN1 (Can be used for Wakeup)
GPIO_26	IO	Programmable I/O 26: GPIO3 PIN2 (Can be used for Wakeup)
GPIO_27	IO	Programmable I/O 27: GPIO3 PIN3 (Can be used for Wakeup)
GPIO_28	IO	Programmable I/O 28: GPIO3 PIN4
GPIO_29	IO	Programmable I/O 29: GPIO3 PIN5
GPIO_30	IO	Programmable I/O 30: GPIO3 PIN6 (Can be used for Wakeup)
GPIO_31	IO	Programmable I/O 31: GPIO3 PIN7
I^2C		
I2C0_DATA	In/OD	I2C0 data
I2C0_CLK	In/OD	I2C0 clock
I2C1_DATA	In/OD	I2C1 data
I2C1_CLK	In/OD	I2C1 clock
I2C2_DATA	In/OD	I2C2 data
I2C2_CLK	In/OD	I2C2 clock
UART		
UA0_RXD	In	UART0 serial data input
UA0_TXD	Out	UART0 serial data output
UA0_RTS_N	Out	UART0 RTS output
UA0_CTS_N	In	UART0 CTS input
UA1_RXD	In	UART1 serial data input
UA1_TXD	Out	UART1 serial data output
UA1_RTS_N	Out	UART1 RTS output
UA1_CTS_N	In	UART1 CTS input
UA2_RXD	In	UART2 serial data input
UA2_TXD	Out	UART2 serial data output
UA2_RTS_N	Out	UART2 RTS output
UA2_CTS_N	In	UART2 CTS input
SPIM		
SPIM0_CS_N	Out	SPIM0 chip select
SPIM0_CLK	Out	SPIM0 clock output
SPIM0_MOSI	Out	SPIM0 serial output
SPIM0_MISO	In	SPIM0 serial input
SPIM1_CS_N	Out	SPIM1 chip select
SPIM1_CLK	Out	SPIM1 clock output
SPIM1_MOSI	Out	SPIM1 serial output
SPIM1_MISO	In	SPIM1 serial input

Function name	I/O	Explanation
SPIM2_CS_N	Out	SPIM2 chip select
SPIM2_CLK	Out	SPIM2 clock output
SPIM2_MOSI	Out	SPIM2 serial output
SPIM2_MISO	In	SPIM2 serial input
SPIM3_CS_N	Out	SPIM3 chip select
SPIM3_CLK	Out	SPIM3 clock output
SPIM3_MOSI	Out	SPIM3 serial output
SPIM3_MISO	In	SPIM3 serial input
SPIC		
SPIC_CS_N	Out	SPIC chip select
SPIC_CLK	Out	SPIC clock output
SPIC_MOSI	IO	SPIC serial output
SPIC_MISO	IO	SPIC serial input
SPIC_IO2	IO	SPIC IO2
SPIC_IO3	IO	SPIC IO3
ADC		
ADC24_SYNC	Out	ADC24 Sampling timing sync output
PWM CAPTURE		
PWM0	Out	ADVTMR PWM output 0
PWM1	Out	ADVTMR PWM output 1
PWM2	Out	ADVTMR PWM output 2
PWM3	Out	ADVTMR PWM output 3
CAPTURE0	In	ADVTMR Capture input 0
CAPTURE1	In	ADVTMR Capture input 1
CAPTURE2	In	ADVTMR Capture input 2
CAPTURE3	In	ADVTMR Capture input 3
TRACE		
TRACECLK	Out	ARM CPU Core TRACECLK
TRACEDATA[0]	Out	ARM CPU Core TRACEDATA[0]
TRACEDATA[1]	Out	ARM CPU Core TRACEDATA[1]
TRACEDATA[2]	Out	ARM CPU Core TRACEDATA[2]
TRACEDATA[3]	Out	ARM CPU Core TRACEDATA[3]

7. Electrical Specification

All the characteristic data indicated in this section are based on design simulation and characterization. They are not tested in production unless otherwise specified.

All characteristics indicated in this section are applicable to the following conditions unless otherwise specified.

- VDD33 = 2.1 to 3.6 V
- AVDD33 = 2.0 to 3.6 V
- VDDC = 0.85 to 1.25 V
- Ta = -20 to 70°C

7.1. Absolute Maximum Ratings

7.1.1. MCU Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

Parameter	Symbol	Pin	Rating	Unit
Supply Voltage	VDDMAX	MCU_VDD33 MCU_VDD33_USB MCU_AVDD33_ADC	-0.3 to 3.9	V
		MCU_VDD12D	-0.3 to 1.6	V
Input Voltage	VINMAX	5 V Tolerant pin (MCU_GPIO0)	-0.3 to MCU_VDD33 + 3.5 or -0.3 to 5.5 (*1)	V
		Other pins	-0.3 to MCU_VDD33 + 0.3 or -0.3 to 3.9 (*1)	V
Input Current	IINMAX	All pins	±10	mA
Storage Temperature	Tstg	—	-40 to 125	°C

*1: Smaller value is applied.

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these ratings would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause breakdown, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

7.1.2. BLE Absolute Maximum Ratings

Maximum ratings must not be exceeded even for a moment. Voltages, currents, and temperatures that exceed the maximum ratings can cause break-downs, degradations, and damages not only for ICs but also for other components and boards. Please make sure application designs not to exceed the maximum ratings in any situation.

Table 7.2 Absolute Maximum Ratings of BLE (VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

item	Symbol	Rating		Unit
		Min	Max	
Supply voltage	BLE_VDD33 BLE_VDDIO (*1)	-0.3	+3.9	V
Input voltage	VIN	-0.3	VDDIO + 0.3	V
Output voltage	VOUT	-0.3	VDDIO + 0.3	V
Input current	IIN	-10	+10	mA
Input power	RFIO	—	+6	dBm
Storage temperature	Tstg	-40	+125	°C

*1: It is not supposed that BLE_VDD33 is grounded while BLE_VDDIO is supplied. It can trigger current path from BLE_VDDIO to BLE_VDD33 through internal circuitry, and may cause degradations and break-downs.

7.2. Operating Ranges

7.2.1. MCU Operating Ranges

Table 7.3 MCU Operating Ranges

Parameter	Symbol	Pin	Condition	Min	Typ.	Max	Unit
Supply Voltage	VDD33	MCU_VDD33	—	2.1	3.3	3.6	V
	AVDD33	MCU_AVDD33_ADC	—	2.0	3.3	3.6	V
	VDD33_USB	MCU_VDD33_USB	—	3.0	3.3	3.6	V
	VDD12	MCU_VDD12D (*1)	Voltage Mode A	1.15	1.2	1.25	V
			Voltage Mode B	1.05	1.1	1.15	
			Voltage Mode C	0.95	1.0	1.05	
Input Clock Frequency	f_{OSCH}	MCU_XIN12M MCU_XOUT12M	—	—	12	—	MHz
	f_{OSCL}	MCU_XIN32K MCU_XOUT32K	—	—	32.768	—	kHz
Operating Temperature	Ta	—	—	-20	25	70	°C

*1: Should be connected to the regulator output pin (MCU_DCDCOUT) with inductor.

7.2.2. BLE Operating Ranges

Table 7.4 BLE Operating Ranges (VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Item	Symbol	Rating			Unit
		Min	Typ.	Max	
Supply voltage	BLE_VDD33 operating voltage	1.8	3.0	3.6	V
	BLE_VDD33 starting voltage	1.96	3.0	3.6	V
	BLE_VDDIO	1.8	3.0	3.6	V
	BLE_VDD15IN	1.45	1.5	3.6	V
	BLE_VDD12A1 BLE_VDD12A2BLE_VDD12X (*1)	—	1.2	—	V
	BLE_VDD12D (*1)	—	1.1	—	V
Frequency range	fc	2400	—	2483.5	MHz
Input frequency	fck	25.99870	26.00000	26.00130	MHz
	fslclk	32.751616	32.768000	32.784384	kHz

*1: No power supply to BLE_VDD12A1, BLE_VDD12A2, BLE_VDD12D and BLE_VDD12X. The power is supplied from the internal regulator.

7.2.3. Internal Power Supply and Power Output

Table 7.5 Internal Power Supply and Power Output

Parameter	Symbol	Condition	Typ.	Unit
MCU Internal Logic Power	VDDC	Voltage Mode A	1.2	V
		Voltage Mode B	1.1	V
		Voltage Mode C	1.0	V
		Voltage Mode D	0.9	V
Power Supply for NOR Flash chip (*1)	VDD18_SPIF	BOOTMODE3 = 0 (Internal LDO supply the power)	1.8	V
		BOOTMODE3 = 1 (MCU_VDD33 pin supply the power)	VDD33	V

*1: Corresponding pins on the package is for the observation of the voltage. Do not use these pins for power supply of external devices.

7.2.4. Internal Clock Frequency

Table 7.6 Internal Clock Frequency

Parameter	Symbol	Condition	Max	Unit
CPU clock AHB Bus clock	fCPU	Clock for CPU, AHB Bus, and AHB bus peripherals (CPU, SRAMC, SPIC, AESA, RNG, EVM)	48	MHz
CPU Trace clock	fCPUTR	Clock for CPU Trace I/F	12	MHz
CPU SysTick clock	fCPUST	Clock for CPU SysTick Timer	12	MHz
APB0 clock	fAPB0	Clock for APB0 Bus and APB0 peripherals (GPIO, TMR, WDT, ADVTMR, I2C2, SPIM2, SPIM3, GCONF, ADC12, ADC24)	12	MHz
APB1 clock	fAPB1	Clock for APB1 Bus and APB1 peripherals (UART0, UART1, I2C0, I2C1, SPIM0, SPIM1)	12	MHz
APB2 clock	fAPB2	Clock for APB2 Bus and APB2 peripherals (UART2)	12	MHz
SPIC clock	fSPIC	Clock for SPIC	48	MHz
USB clock	fUSB	Clock for USB	48	MHz
UART0 clock	fUA0	Clock for baud rate of UART0	18	MHz
UART1 clock	fUA1	Clock for baud rate of UART1	18	MHz
UART2 clock	fUA2	Clock for baud rate of UART2	18	MHz
ADC12 clock	fAD12	Clock for ADC12	12	MHz
ADC24 clock	fAD24	Clock for ADC24	4	MHz
RTC	fRTC	Clock for RTC	32.768	kHz

7.3. Power Consumption

7.3.1. MCU Power Consumption

The current consumption value indicated in Table 7.7 is measured with the condition below:

- VDD33 = 3.3 V
- All ACTIVE State current consumptions are measured with CoreMark™ benchmark program.
- The program is loaded to SRAM from SPIC, and CPU fetched the codes and data from SRAM during running the benchmark.
- Basically, clocks of CPU, buses, SRAMC, PMU and RTC are supplied, and clocks of other peripherals are stopped. PEFUSE domain, PF domain and PU domain are powered-off unless otherwise specified.
- Dynamic Clock Gating function implemented in PMU is enabled.
- In WAIT-RETNTION State, only PA domain and PM domain are powered and other domains are powered-off or in retention state.
- In RTC and STOP mode, only PA domain is powered.
- In WAIT, WAIT-RETENTION, RETENTION and RTC mode, all clock sources except 32.768 kHz for RTC are disabled. In STOP mode, all clock sources including 32.768 kHz clock are disabled.

Other specific conditions are described in the table.

Table 7.7 Current Consumption for each Power Mode (VDD33 = 3.3V, Ta = 25°C)

Power Mode	Voltage Mode	Conditions	Typ.	Max	Unit
ACTIVE	A	48 MHz (Clock Source: PLL, OSC12M used), DCDC 1.2 V	3.1	3.5	mA
	B	36 MHz (Clock Source: PLL, OSC12M used), DCDC 1.1 V	2.3	2.6	mA
	C	12 MHz (Clock Source: OSC12M, PLL disabled), DCDC 1.0 V	1.1	1.5	mA
	D	4 MHz (Clock Source: SIOSC4M, PLL and OSC12M disabled), LDOS 0.9 V	0.6	0.7	mA
SLEEP0	A	48 MHz (Clock Source: PLL, OSC12M used), DCDC 1.2 V	1.3	1.8	mA
	B	36 MHz (Clock Source: PLL, OSC12M used), DCDC 1.1 V	1.1	1.5	mA
	C	12 MHz (Clock Source: OSC12M, PLL disabled), DCDC 1.0 V	0.8	1.0	mA
	D	4 MHz (Clock Source: SIOSC4M, PLL and OSC12M disabled), LDOS 0.9 V	0.3	0.4	mA
SLEEP1	A	48 MHz (Clock Source: PLL, OSC12M used), DCDC 1.2 V	1.3	1.8	mA
	B	36 MHz (Clock Source: PLL, OSC12M used), DCDC 1.1 V	1.1	1.5	mA
	C	12 MHz (Clock Source: OSC12M, PLL disabled), DCDC 1.0 V	0.8	1.0	mA
	D	4 MHz (Clock Source: SIOSC4M, PLL and OSC12M disabled), LDOS 0.9 V	0.3	0.4	mA
SLEEP2	A	48 MHz (Clock Source: PLL, OSC12M used), DCDC 1.2 V	1.1	1.6	mA
	B	36 MHz (Clock Source: PLL, OSC12M used), DCDC 1.1 V	1.0	1.3	mA
	C	12 MHz (Clock Source: OSC12M, PLL disabled), DCDC 1.0 V	0.7	0.9	mA

Power Mode	Voltage Mode	Conditions	Typ.	Max	Unit
	D	4 MHz (Clock Source: SIOSC4M, PLL and OSC12M disabled), LDOS 0.9 V	0.2	0.3	mA
WAIT	D	LDOS 0.9 V	15.8	27.7	μA
WAIT-RETENTION	D	LDOS 0.9 V	12.4	23.4	μA
RETENTION	D	LDOS 0.9 V	5.4	9.0	μA
RTC	D	LDOS 0.9 V	3.2	4.8	μA
STOP	D	LDOS 0.9 V	1.5	2.9	μA

7.3.2. BLE Power Range

The current consumption characteristics are shown in the following table. The values are the average current values under the circumstances in TOSHIBA recommended power connections, and the ambient temperature of 25°C.

Table 7.8 Current Consumption (VDD = VDDIO = 3.0 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V, DCDCEN = VDD)

Item	Symbol	Conditions	Measuring port	Rating			Unit
				Min	Typ.	Max	
Digital circuit operation 26 MHz/32.768 kHz clocks are supplied. Internal CPU 13 MHz operation Peak current consumption	IDDDIG (Active1)	—	VDD	—	1.9	—	mA
Data reception Peak current consumption	IDDRX (Active3)	—	VDD	—	6.3	—	
Data transmission Peak current consumption	IDDTX (Active3)	Output Power = -4 dBm	VDD	—	6.3	—	
Current consumption in Low power mode With Connection No XOIN supply SLEEPCLK is supplied.	IDDS1 (Sleep)	—	VDD	—	10.5	—	μA
Current consumption in Low power mode Without Connection No XOIN supply SLPXOIN is supplied.	IDDS2 (Backup)	—	VDD	—	5.0	—	
Current consumption in Low power mode Without Connection No XOIN supply No SLPXOIN supply.	IDDDS (Deep Sleep)	—	VDD	—	0.1	—	

7.4. DC Characteristics

Table 7.9 to Table 7.12 shows DC characteristics of IO pins. Regarding correspondence between each pin and IO cell type, please see signal list described in Section 4.

7.4.1. Schmitt Level Input / Multi-Drive Output / Programmable Pull-Up/Down IO pins

Table 7.9 Schmitt Level Input / Multi-Drive Output / Programmable Pull-Up/Down IO characteristics

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Low-level input current	IIL	VIN = VSS	Pull-up Disable	-10	—	10	µA
		VIN = VSS	Pull-up Enable (PUX=0)	-200	—	-10	µA
High-level input current	IIH	VIN = VDD33	Pull-down Disable	-10	—	10	µA
		VIN = VDD33	Pull-down Enable (PDX=0)	10	—	200	µA
Low-level input voltage	VIL	—	—	—	—	VDD33 × 0.3	V
High-level input voltage	VIH	—	—	VDD33 × 0.7	—	—	V
Low-level output voltage	VOL	VDD33 = 2.8 to 3.6 V	{CTL2,CTL1} = 00 (*1) IOL = 2 mA	—	—	0.4	V
			{CTL2,CTL1} = 01 (*1) IOL = 4 mA	—	—	0.4	V
			{CTL2,CTL1} = 10 (*1) IOL = 6 mA	—	—	0.4	V
			{CTL2,CTL1} = 11 (*1) IOL=8 mA	—	—	0.4	V
		VDD33 = 2.1 to 2.8 V	{CTL2,CTL1} = 00 (*1) IOL = 1.5 mA	—	—	0.4	V
			{CTL2,CTL1} = 01 (*1) IOL = 3 mA	—	—	0.4	V
			{CTL2,CTL1} = 10 (*1) IOL = 4.5 mA	—	—	0.4	V
			{CTL2,CTL1} = 11 (*1) IOL = 6 mA	—	—	0.4	V
High-level output voltage	VOH	VDD33 = 2.8 to 3.6 V	{CTL2,CTL1} = 00 (*1) IOH = -2 mA	VDD33 -0.4	—	—	V
			{CTL2,CTL1} = 01 (*1) IOH = -4 mA	VDD33 -0.4	—	—	V
			{CTL2,CTL1} = 10 (*1) IOH = -6 mA	VDD33 -0.4	—	—	V
			{CTL2,CTL1} = 11 (*1) IOH = -8 mA	VDD33 -0.4	—	—	V
		VDD33 = 2.1 to 2.8 V	{CTL2,CTL1} = 00 (*1) IOH = -1.5 mA	VDD33 -0.4	—	—	V
			{CTL2,CTL1} = 01 (*1) IOH = -3 mA	VDD33 -0.4	—	—	V
			{CTL2,CTL1} = 10 (*1) IOH = -4.5 mA	VDD33 -0.4	—	—	V
			{CTL2,CTL1} = 11 (*1) IOH = -6 mA	VDD33 -0.4	—	—	V

*1: CTL2, CTL1 is a control register of GCONF block. Please see the GCONF section of the reference manual for detail.

Typical characteristics of output current (IOL/IOH) is shown on the figure below.

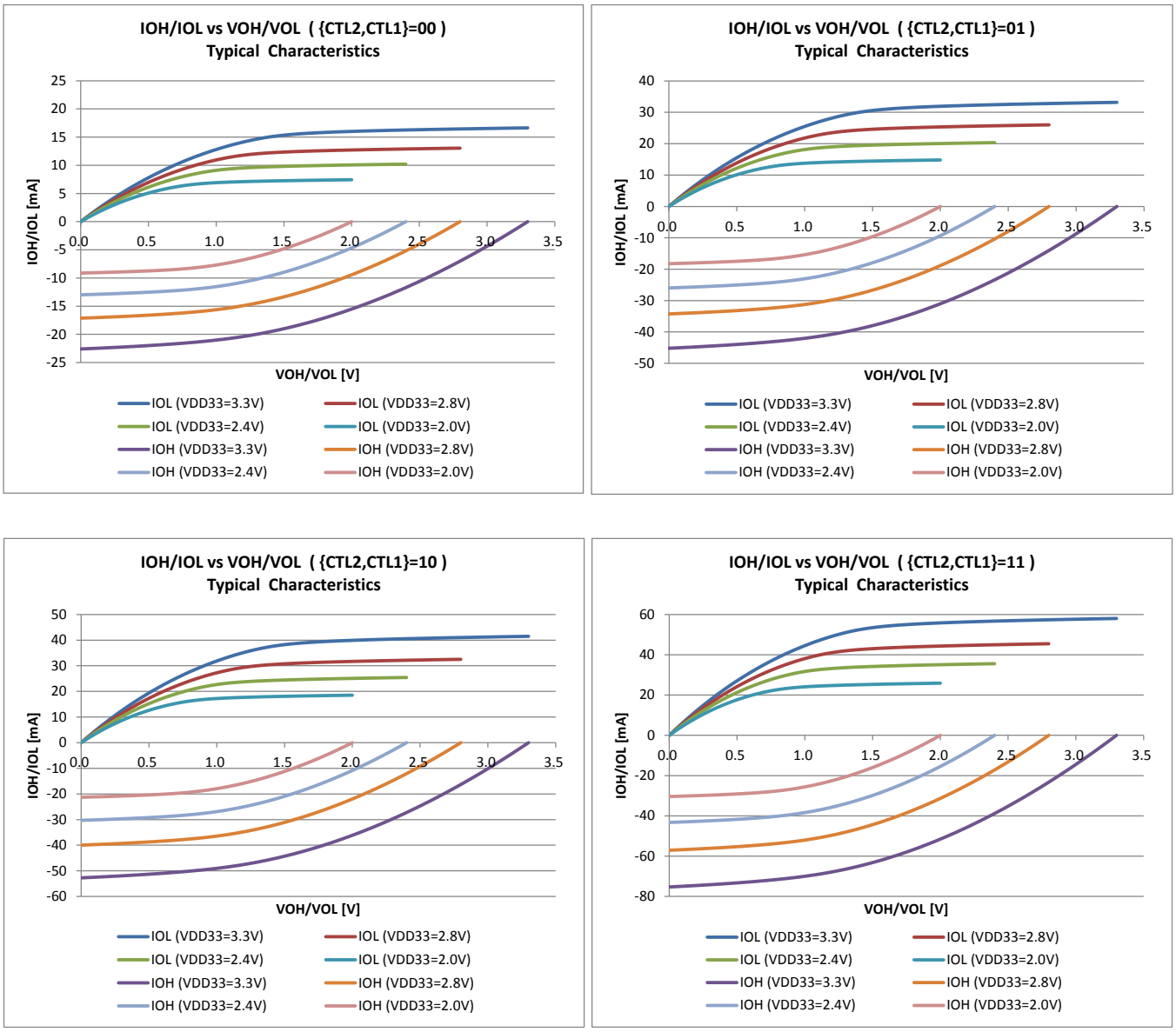


Figure 7.1 IOL/IOH Typical Characteristics

7.4.2. Schmitt Level Input only pin

Table 7.10 Schmitt Level Input only pin characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Low-level input current	IIL	VIN = VSS	-10	—	10	μA
High-level input current	IIH	VIN = VDD33	-10	—	10	μA
Low-level input voltage	VIL	—	—	—	VDD33 × 0.35	V
High-level input voltage	VIH	—	VDD33 × 0.7	—	—	V

7.4.3. 5 V Tolerant Schmitt Level only Input pin

Table 7.11 5 V Tolerant Schmitt Level Input only pin characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Low-level input current	IIL	VIN = VSS	-10	—	10	μA
High-level input current	IIH	VIN = VDD33	-10	—	10	μA
Low-level input voltage	VIL	—	—	—	VDD33 × 0.3	V
High-level input voltage	VIH	—	VDD33 × 0.7	—	—	V

7.4.4. Output only pin

Table 7.12 Output only pin characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Low-level output voltage	VOL	VDDIO = 2.8 to 3.6 V, IOL = 2 mA	—	—	0.4	V
		VDDIO = 2.1 to 2.8 V, IOL = 1.5 mA	—	—	0.4	V
High-level output voltage	VOH	VDDIO = 2.8 to 3.6 V, IOH = -2 mA	VDD33 - 0.4	—	—	V
		VDDIO = 2.1 to 2.8 V, IOH = -1.5 mA	VDD33 - 0.4	—	—	V

7.4.5. BLE DC Characteristics

Table 7.13 DC Characteristics (VDD = VDDIO = 3.0 V, VSSD = VSSA1 = VSSA2 = VSSX = 0 V)

Item	Symbol	Condition		Measuring port	Rating			Unit
		I/F Voltage	Other Condition		Min	Typ.	Max	
High-level input voltage	VIH	3.0 V	LVCMOS	VDDIO	0.8 × VDDIO	—	—	V
Low-level input voltage	VIL	3.0 V	LVCMOS	VDDIO	—	—	0.2 × VDDIO	V
High-level input current	IIH	VDDIO = Input Voltage of each pin	Pull-down Off	VDDIO	-10	—	10	µA
			Pull-down On		10	—	200	
Low-level input current	IIL		Pull-up Off		-10	—	10	
			Pull-up On		-200	—	-10	
High-level output voltage	VOH	3.0 V	IOH = 1 mA	VDDIO	VDDIO - 0.6	—	—	V
Low-level output voltage	VOL	3.0 V	IOL = 1 mA	VDDIO	—	—	0.4	V
External 32.768 kHz clock input level (*1)	VIH SLPCLK	3.0 V	—	SLPXOOUT	0.8 × VDDIO	—	—	V
	VIL SLPCLK	3.0 V	—	SLPXOOUT	—	—	0.2 × VDDIO	V

*1: In case of using an external oscillator, when can't use a crystal oscillator.

7.5. Clock Source Characteristics

7.5.1. XOSC12M

Table 7.14 XOSC12M characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fO12M	—	—	12	—	MHz
External Feedback Resistor (*1)	Rf	—	—	1	—	MΩ
External Load Capacitance (*1)	CL	Assume equivalent series resistance Rs is about 50 to 60 Ω	—	8	—	pF
Startup Time	tSTART	OVERRIDE_EFUSE_OSC12M_ MAIN_GM = 0b0000 (*2)	—	—	1	ms

*1: The value is based on simulation result obtained with typical external components parameter. The value of these parameters varies depending on the crystal resonator used. It is recommended to refer the datasheet of the crystal resonator that you are going to use.

*2: OVERRIDE_EFUSE_OSC12M_MAIN_GM is one of the fields of the control register *[OVERRIDE_EFUSE_OSC12M]* in Power Management Unit (PMU). Please see the PMU section of the reference manual for detail. Changing these bit results in changing of the startup time

7.5.2. XOSC32K

Table 7.15 XOSC32K characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fO32K	—	—	32.768	—	kHz
External Feedback Resistor (*1)	Rf	—	—	10	—	MΩ
External Load Capacitance (*1)	CL	Assume equivalent series resistance Rs is about 50 to 55 kΩ	—	12.5	—	pF
Startup Time	tSTART	—	—	—	1000	ms
Frequency stabilization after Boost disable.	tSTBL	—	—	—	2	ms

*1: The value is based on simulation result obtained with typical external components parameter. The value of these parameters varies depending on the crystal resonator used. It is recommended to refer the datasheet of the crystal resonator that you are going to use.

7.5.3. SIOSC4M

Table 7.16 SIOSC4M characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fSO4M	Trimmed to default Voltage Mode (Mode A)	3.7	4.0	4.2	MHz
		Trimmed to each Voltage Mode	3.86	4.0	4.14	MHz
Startup Time	tSTASO4M	—	—	—	6	cycle

*1: When SIOSC4M is used for the source clock of the peripherals, take into consideration the variation in frequency.

7.5.4. SIOSC32K

Table 7.17 SIOSC32K characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fSO32K	—	29.982	32.768	35.554	kHz
Startup Time	tSTASO32K	—	—	—	500	µs

7.5.5. PLL

Table 7.18 PLL characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Output Clock Frequency	fCK	ND = 11 (*1)	—	48	—	MHz
		ND = 10 (*1)	—	36	—	MHz
		ND = 01 (*1)	—	24	—	MHz
Reference Input Frequency	fFN	—	—	12	—	MHz
Lockup Time	tLU	—	—	—	100	µs

7.5.6. ADPLL

Table 7.19 ADPLL characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Output Clock Frequency	fCK	—	—	47.972	—	MHz
Reference Input Frequency	fFN	—	—	32.768	—	kHz
Lockup Time	tLU	Normal Mode	—	—	8000	µs
		High-Speed Lockup Mode (*1)	—	—	2000	µs
Standby Return Time	tSR	—	—	—	2000	µs

*1: Please refer the PMU section of the reference manual to see how to enable High-Speed Lockup Mode.

7.6. Analog Characteristics

7.6.1. LVD

Table 7.20 LVD characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Brown-out Reset Detect Level	VBOR	Default setting	1.6	1.7	1.8	V

7.6.2. BGR

Table 7.21 BGR characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
BGR monitor output signal level	VBGR	—	—	1.24	—	V

7.6.3. DCDC

Table 7.22 DCDC characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Voltage	VOUT	Voltage Mode A	—	1.2	—	V
		Voltage Mode B	—	1.1	—	V
		Voltage Mode C	—	1.0	—	V

7.6.4. LDOF

Table 7.23 LDOF characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Voltage	VOUT	—	—	1.8	—	V

7.6.5. LDOS

Table 7.24 LDOS characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Voltage	VOUT	Mode D	—	0.9	—	V

7.6.6. 12-bit SAR ADC

Table 7.25 12-bit SAR ADC characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resolution	—	—	—	12	—	Bit
Core Clock Frequency	fCLK	—	—	—	12	MHz
Conversion Time (*1)	—	Cycles in Core Clock	—	—	17	Cycles
Top Reference Voltage	VREFH	—	—	—	AVDD33	V
Bottom Reference Voltage	VREFL	—	0	—	—	V
Analog Input Range	VIN	Single-ended Voltage	VREFL	—	VREFH	V
Integral Nonlinearity	INL	—	—	±4	±12	LSB
Differential Nonlinearity	DNL	—	—	±2	±8	LSB
Offset Error	OE	—	—	±4	±16	LSB
Gain Error	GE	—	—	±2	±32	LSB
Operating Current (*2)	IDD	—	—	1.0	—	mA
Standby Current (*2)	IDDS	—	—	0.1	—	μA

*1: Required clock cycle of ADC core. Setup cycles of control logic are not included.

*2: The current of AVDD33 power supply.

7.6.7. 24-bit ΔΣ A/D converter

Table 7.26 24-bit ΔΣ ADC characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resolution	—	—	—	24	—	Bit
Core Clock Frequency	fCLK	—	3.8	4	4.2	MHz
Conversion Time (*1) (Cycles in Core Clock)	—	CNT_MODE[1:0] = 00 (*2)	—	—	4130	Cycles
		CNT_MODE[1:0] = 01 (*2)	—	—	1058	
		CNT_MODE[1:0] = 10 (*2)	—	—	546	
		CNT_MODE[1:0] = 11 (*2)	—	—	290	
Top Reference Voltage	VREFH	—	—	—	AVDD33	V
Bottom Reference Voltage	VREFL	—	0	—	—	V
Analog Input Configuration	—	CNT_MODE[11] = 0 (*2)	Differential Voltage			
		CNT_MODE[11] = 1 (*2)	Differential Current			
Analog Input Voltage Range	VIN	Voltage Input Mode	0.1	—	AVDD33-0.1	V
Input Impedance	ZIN	Voltage Input Mode	20	35	—	MΩ
I/V Conversion Resistance	Rf	Current Input Mode	10k	—	1M	Ω
Effective Number of Bit	ENOB	CNT_MODE[1:0] = 00 (*2)	—	19	—	Bit
		CNT_MODE[1:0] = 01 (*2)	—	18	—	
		CNT_MODE[1:0] = 10 (*2)	—	17.5	—	
		CNT_MODE[1:0] = 11 (*2)	—	17	—	
Integral Nonlinearity	INL	Voltage Input Mode, CNT_MODE[1:0] = 00 (*2)	—	±75	±256	LSB
Offset Error	OE	Voltage Input Mode, CNT_MODE[1:0] = 00 (*2)	—	±10	±50	μV
Gain Error	GE	Voltage Input Mode, CNT_MODE[1:0] = 00 (*2)	—	±0.5	±1	%FS
Common mode Rejection Ratio	CMRR	Voltage Input Mode, DC to 120 Hz	60	85	—	dB
Operating Current (*3)	IDD	—	—	1.1	—	mA
Standby Current (*3)	IDDS	—	—	0.1	—	μA

*1: Required clock cycle of ADC core. Setup cycles of control logic are not included.

*2: CNT_MODE is a control register of ADC24 block. Please see the ADC24 section of the reference manual for detail.

*3: The current of AVDD33 power supply.

7.6.8. USB Full Speed IO

Table 7.27 USB FSIO characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Differential Drivers Cross Over Voltage	VCRS	—	1.3	—	2.0	V
Differential Input Sensitivity	VDI	—	200	—	—	mV
Differential Common Mode Range	VCM	—	0.8	—	2.5	V
Single Ended Receiver Input Range	VSER	—	0.8	—	2.0	V
Single Ended Receiver Hysteresis	VSHSYT	—	200	—	—	mV
Input Voltage Low	VIL	—	0.0	—	0.8	V
Input Voltage High	VIH	—	2.0	—	—	V
Output Voltage Low	VOL	—	0.0	—	0.3	V
Output Voltage High	VOH	—	2.8	—	VDD33_USB	V
Full Speed Driver Rise Time	TFR	Rext = 1.5 kΩ, CL = 50 pF (*1)	4	—	20	ns
Full Speed Driver Fall Time	TFF	Rext = 1.5 kΩ, CL = 50 pF (*1)	4	—	20	ns
Full Speed Operating Current (*2)	ICCFS	VDD33_USB = 3.3 V	—	8.5	—	mA
Suspended Supply Current (*2)	ICCS	VDD33_USB = 3.3 V	—	25	—	μA

*1: Figure below illustrates external loading for Full Speed Driver Rise/Fall time.

*2: The current of VDD33_USB power supply.

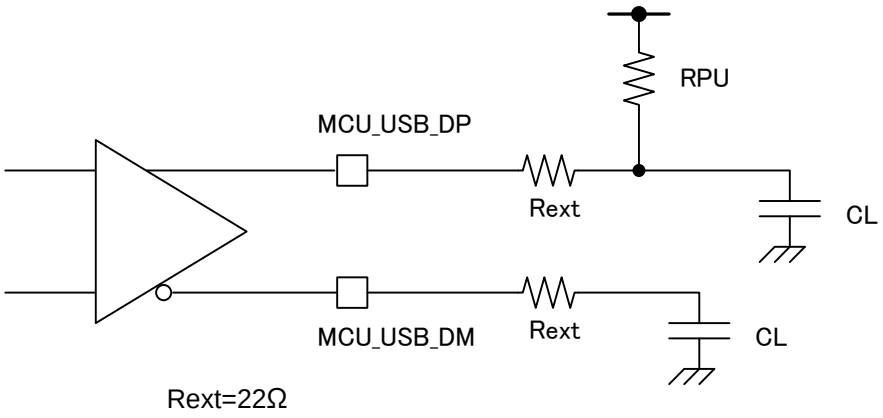


Figure 7.2 External Loading for Full Speed Driver Rise/Fall time

7.7. AC Characteristics

7.7.1. RESET Input

Table 7.28 RESET input timing requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
MCU_SYS_RESET_N assertion time	tRST	—	0.1	—	—	μs

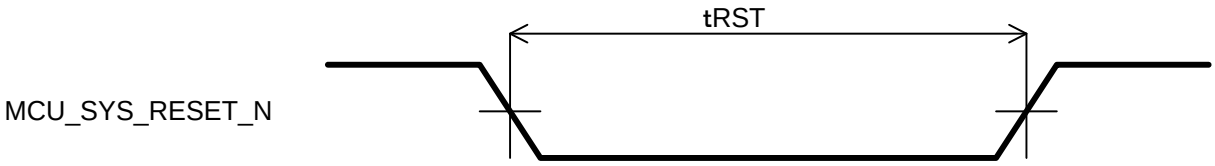


Figure 7.3 RESET input timing

7.7.2. GPIO Input

Table 7.29 GPIO input timing requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
High level assertion time for wakeup (*1)	tHWU	—	0.2	—	—	μs
Low level assertion time for wakeup (*1)	tLWU	—	0.2	—	—	μs

*1: Applied to GPIO30/27/26/25/24/7/6/5/4/3/2/1/0

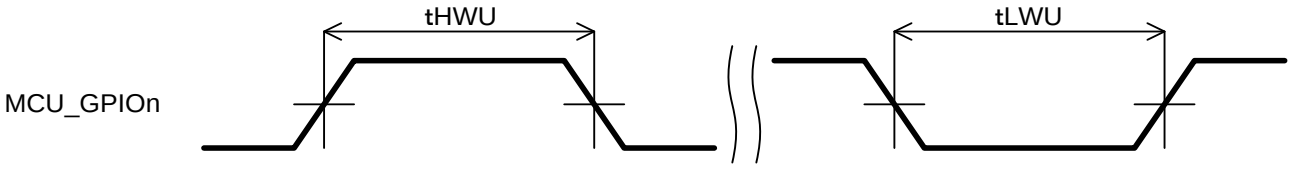


Figure 7.4 GPIO input timing

7.7.3. SPI Interface

Table 7.30 SPI Interface Timing requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
SPI clock frequency	fSPCLK	—	—	—	6	MHz
SPI input data setup time	tSPS	—	63.3	—	—	ns
SPI input data hold time	tSPH	—	0	—	—	ns
SPI output data delay time	tSPD	—	—	—	63.3	ns

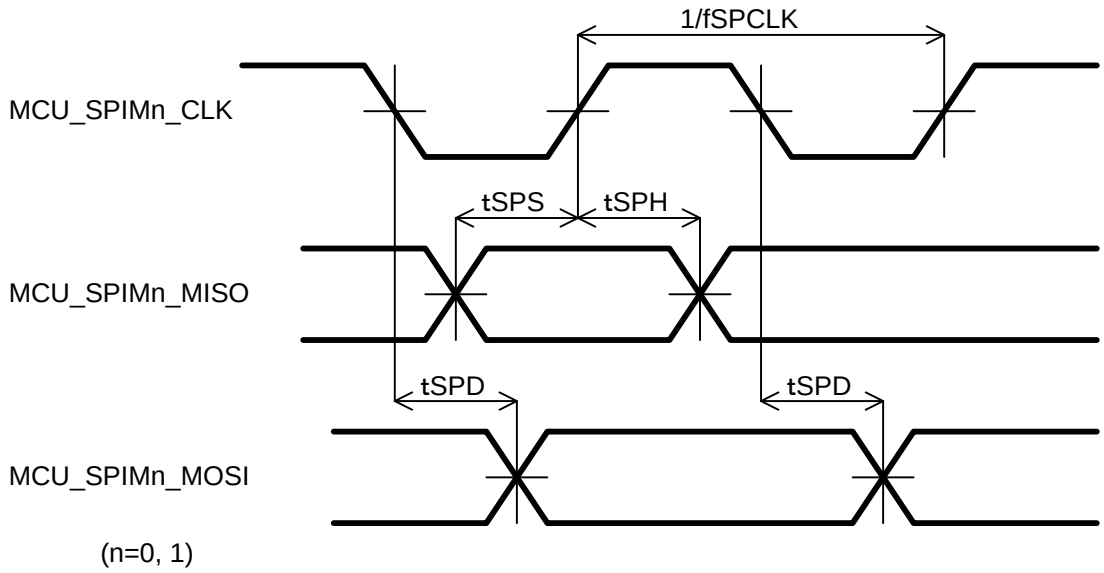


Figure 7.5 SPI Interface Timing

7.7.4. I²C Interface

- Standard Speed (100 kHz)

Table 7.31 I²C Interface Standard Speed (100 kHz) Timing Requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
I²C clock frequency (*1)(*2)	fI2CLK	—	—	—	100	kHz
I²C clock low time (*1)(*2)	tI2LOW	—	4.7	—	—	μs
I²C clock high time (*1)(*2)	tI2HIGH	—	4.0	—	—	μs
I²C clock/data rise time	tI2TR	—	—	—	1000	ns
I²C clock/data fall time	tI2TF	—	—	—	300	ns
I²C data input setup time	tI2DS	—	250	—	—	ns
I²C data input hold time	tI2DH	—	0	—	3.45	μs
capacitive load for each bus line	Cb	—	—	—	400	pF

- Fast Speed (400 kHz)

Table 7.32 I²C Interface Fast Speed (400 kHz) Timing Requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
I²C clock frequency (*1)(*2)	fI2CLK	—	—	—	400	kHz
I²C clock low time (*1)(*2)	tI2LOW	—	1.3	—	—	μs
I²C clock high time (*1)(*2)	tI2HIGH	—	0.6	—	—	μs
I²C clock/data rise time	tI2TR	—	20	—	300	ns
I²C clock/data fall time	tI2TF	—	20 × (VDD33 / 5 V)	—	300	ns
I²C data input setup time	tI2DS	—	100	—	—	ns
I²C data input hold time	tI2DH	—	0	—	0.9	μs
capacitive load for each bus line	Cb	—	—	—	400	pF

*1: Frequency of APB clock (fAPB0 for I2C2 and fAPB1 for I2C0/I2C1) must be at least 4 MHz for Standard mode operation. and at least 12 MHz for Fast mode operation.

*2: Need to proper setting of I²C control register. Please see the I²C section of the reference manual for detail.

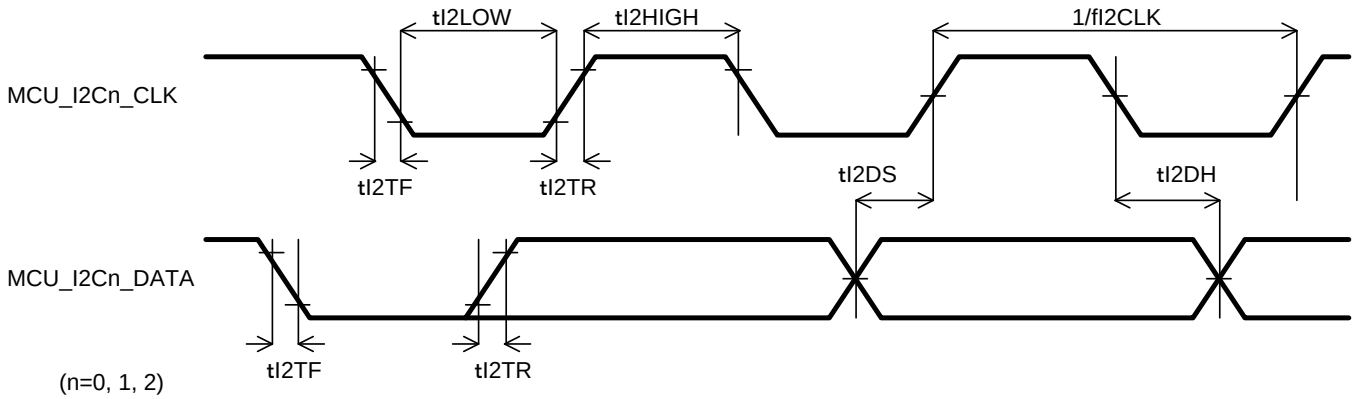


Figure 7.6 I²C Interface Timing

Most of the I²C timing requirements listed in above table needs appropriate setting of I²C control registers. Please see the I²C section of the reference manual for detail.

7.7.5. DEBUG Interface

- JTAG

Table 7.33 JTAG Interface Timing Requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
MCU_DBG_TCK frequency	fTCK	—	100	—	—	ns
DEBUG input data setup time	tDBS	—	20	—	—	ns
DEBUG input data hold time	tDBH	—	15	—	—	ns
DEBUG output data delay time	tDBD	—	4	—	30	ns

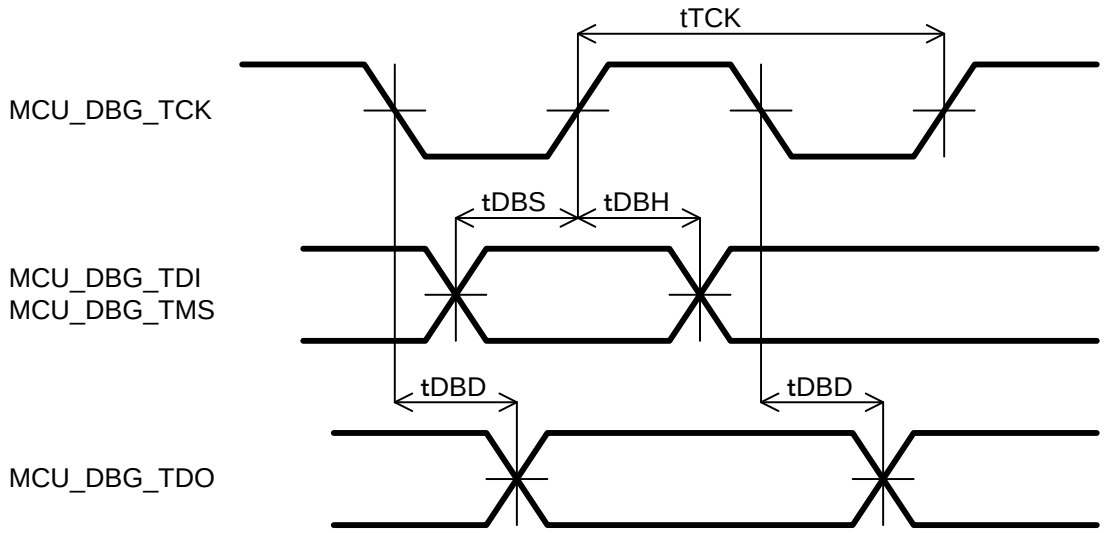


Figure 7.7 JTAG Interface Timing

- Serial Wire

Table 7.34 Serial Wire Interface Timing requirement

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
MCU_DBG_TCK frequency	fSWCK	—	100	—	—	ns
DEBUG input data setup time	tDBS	—	20	—	—	ns
DEBUG input data hold time	tDBH	—	15	—	—	ns
DEBUG output data delay time	tDBD	—	4	—	50	ns

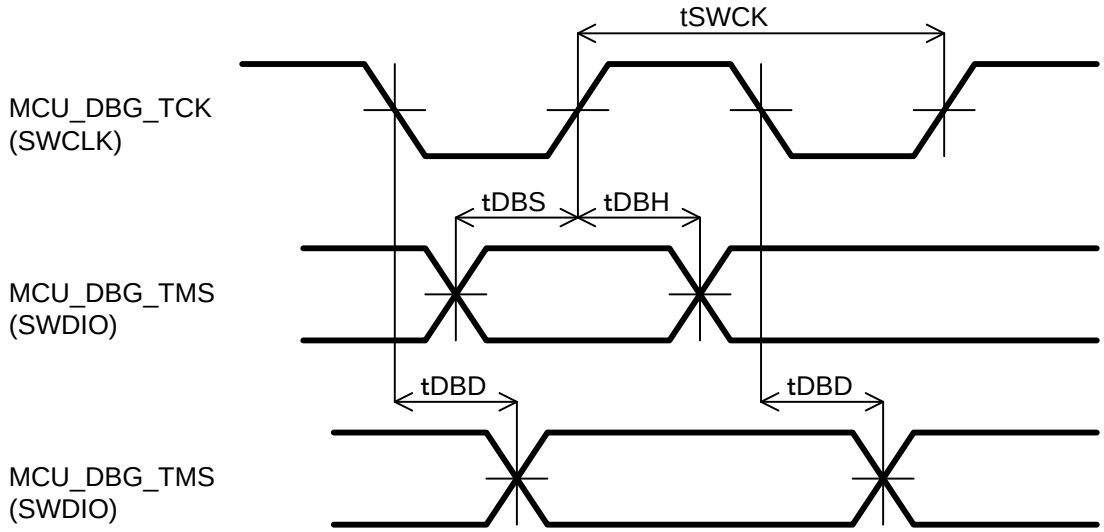


Figure 7.8 Serial Wire Interface Timing

8. Mechanical Characteristics

8.1. Package Drawings

P-LFBGA136-0807-0.50-001 Unit: mm

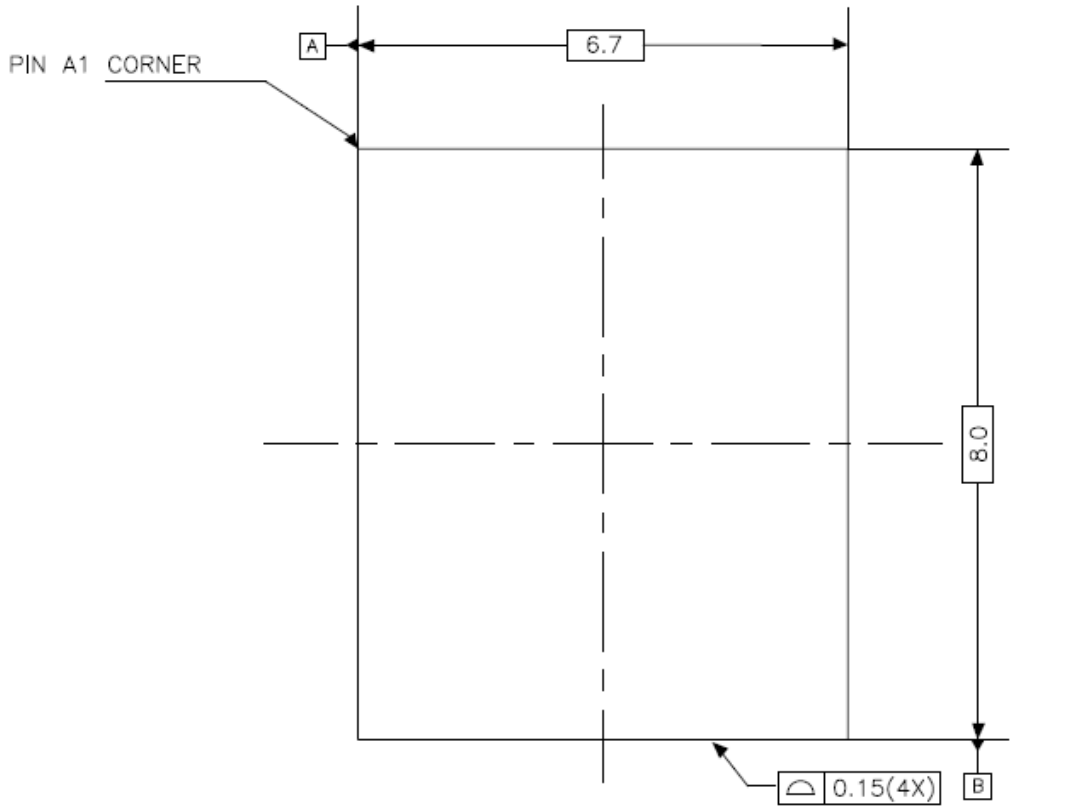


Figure 8.1 Top View

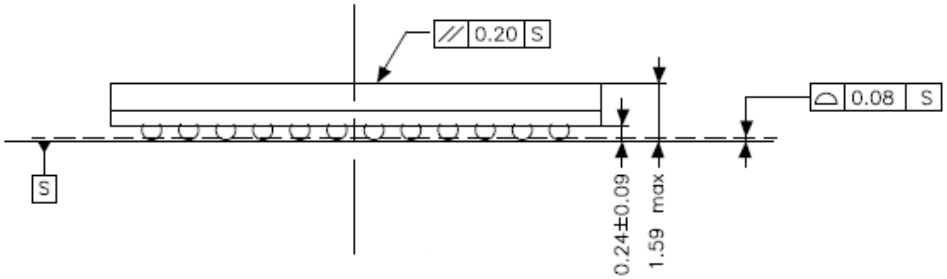
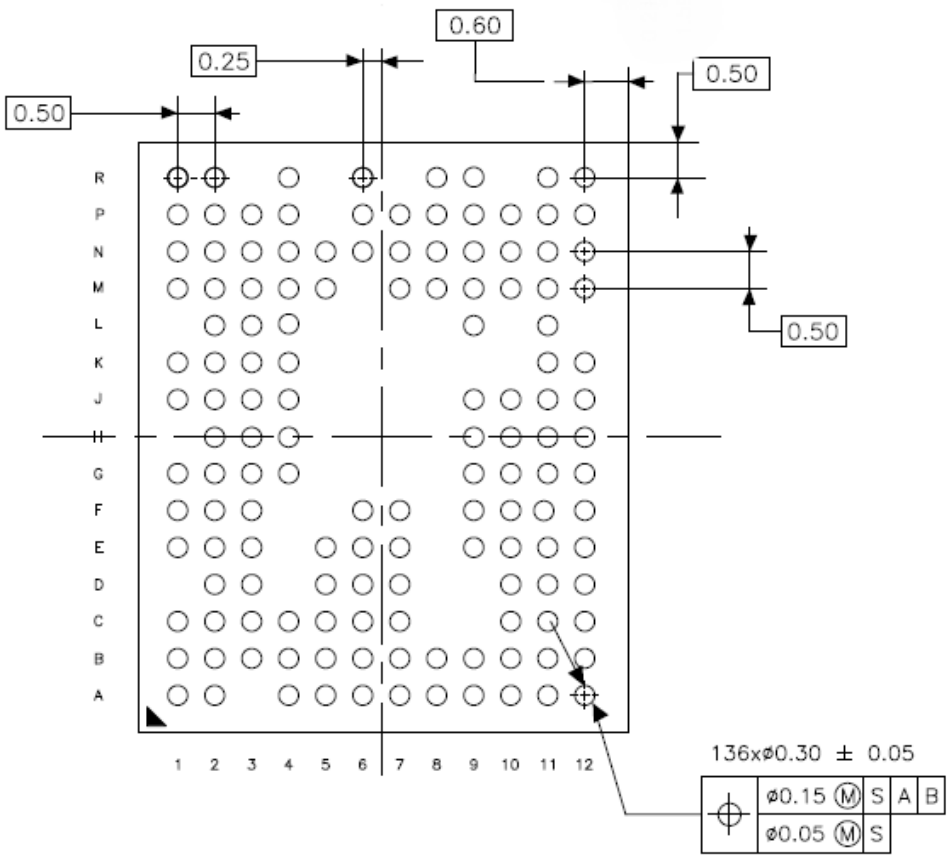


Figure 8.2 Side View

P-LFBGA136-0807-0.50-001 Unit: mm



Weight: 0.16 g (Typ.)

Figure 8.3 Bottom View

Note: Figure 8.1, Figure 8.2 and Figure 8.3 are for explanation. Please contact your TOSHIBA sales representative for the dimensions that are not written on the figures.

9. Revision History

Table 9.1 Revision History

Revision	Date	Description
0.1	2015-08-03	Newly released.
0.2	2015-08-27	Revised Table 7.20 LVD characteristic in Section 7.6.1.
0.3	2015-11-16	Added a note in Section 7.5.3. Deleted a note in Table 7.20.
1.0	2016-01-15	Changed description from chapter number to reference manual title. Official version.

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